

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction tests for VRR-c encoded:
				5 *
				6 * E760 VMRL - Vector Merge Low
				7 * E761 VMRH - Vector Merge High
				8 * E794 VPK - Vector Pack
				9 *
				10 * James Wekel March 2025
				11 *****
				13 *****
				14 *
				15 * basic instruction tests
				16 *
				17 *****
				18 * This program tests proper functioning of the z/arch E7 VRR-c vector
				19 * merge (high and low) and pack instructions.
				20 *
				21 * Exceptions are not tested.
				22 *
				23 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				24 * obvious coding errors. None of the tests are thorough. They are
				25 * NOT designed to test all aspects of any of the instructions.
				26 *
				27 *****
				28 *
				29 * *Testcase zvector-e7-14-MergePack
				30 * *
				31 * * Zvector E7 instruction tests for VRR-c encoded:
				32 * *
				33 * * E760 VMRL - Vector Merge Low
				34 * * E761 VMRH - Vector Merge High
				35 * * E794 VPK - Vector Pack
				36 * *
				37 * * # -----
				38 * * # This tests only the basic function of the instructions.
				39 * * # Exceptions are NOT tested.
				40 * * # -----
				41 * *
				42 * main size 2
				43 * numcpu 1
				44 * sysclear
				45 * archlvl z/Arch
				46 * *
				47 * loadcore "\$(testpath)/zvector-e7-14-MergePack.core" 0x0
				48 * *
				49 * diag8cmd enable # (needed for messages to Hercules console)
				50 * runtest 5
				51 * diag8cmd disable # (reset back to default)
				52 * *
				53 * *Done
				54 * *
				55 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				57 *****
				58 * FCHECK Macro - Is a Facility Bit set?
				59 *
				60 * If the facility bit is NOT set, an message is issued and
				61 * the test is skipped.
				62 *
				63 * Fcheck uses R0, R1 and R2
				64 *
				65 * eg. FCHECK 134, 'vector-packed-decimal'
				66 *****
				67 MACRO
				68 FCHECK &BITNO, &NOTSETMSG
				69 . * &BITNO : facility bit number to check
				70 . * &NOTSETMSG : 'facility name'
				71 LCLA &FBBYTE Facility bit in Byte
				72 LCLA &FBBIT Facility bit within Byte
				73
				74 LCLA &L(8)
				75 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				76
				77 &FBBYTE SETA &BITNO/8
				78 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				79 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				80
				81 B X&SYSNDX
				82 * Fcheck data area
				83 * skip messgae
				84 SKT&SYSNDX DC C' Skipping tests: '
				85 DC C&NOTSETMSG
				86 DC C' (bit &BITNO) is not installed.'
				87 SKL&SYSNDX EQU *-SKT&SYSNDX
				88 * facility bits
				89 DS FD gap
				90 FB&SYSNDX DS 4FD
				91 DS FD gap
				92 *
				93 X&SYSNDX EQU *
				94 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				95 STFLE FB&SYSNDX get facility bits
				96
				97 XGR R0, R0
				98 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				99 N R0, =F' &FBBIT' is bit set?
				100 BNZ XC&SYSNDX
				101 *
				102 * facility bit not set, issue message and exit
				103 *
				104 LA R0, SKL&SYSNDX message length
				105 LA R1, SKT&SYSNDX message address
				106 BAL R2, MSG
				107
				108 B EOJ
				109 XC&SYSNDX EQU *
				110 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				112	*****		
				113	* Low core PSWs		
				114	*****		
00000000		00000000	00002B9F	115	ZVE7TST START 0		
		00000000		116	USING ZVE7TST, R0	Low core addressability	
		00000140	00000000	117			
				118	SVOLDPSW EQU ZVE7TST+X' 140'	z/Arch Supervisor call old PSW	
00000000		00000000	000001A0	120	ORG ZVE7TST+X' 1A0'	z/Architecture RESTART PSW	
000001A0	00000001 80000000			121	DC X' 0000000180000000'		
000001A8	00000000 00000200			122	DC AD(BEGIN)		
000001B0		000001B0	000001D0	124	ORG ZVE7TST+X' 1D0'	z/Architecture PROGRAM CHECK PSW	
000001D0	00020001 80000000			125	DC X' 0002000180000000'		
000001D8	00000000 0000DEAD			126	DC AD(X' DEAD')		
000001E0		000001E0	00000200	128	ORG ZVE7TST+X' 200'	Start of actual test program..	
				130	*****		
				131	* The actual "ZVE7TST" program itself...		
				132	*****		
				133	*		
				134	* Architecture Mode: z/Arch		
				135	* Register Usage:		
				136	*		
				137	* R0 (work)		
				138	* R1-4 (work)		
				139	* R5 Testing control table - current test base		
				140	* R6- R7 (work)		
				141	* R8 First base register		
				142	* R9 Second base register		
				143	* R10 Third base register		
				144	* R11 E7TEST call return		
				145	* R12 E7TESTS register		
				146	* R13 (work)		
				147	* R14 Subroutine call		
				148	* R15 Secondary Subroutine call or work		
				149	*		
				150	*****		
00000200		00000200		152	USING BEGIN, R8	FIRST Base Register	
00000200		00001200		153	USING BEGIN+4096, R9	SECOND Base Register	
00000200		00002200		154	USING BEGIN+8192, R10	THIRD Base Register	
00000200	0580			156	BEGIN BALR R8, 0	Inititalize FIRST base register	
00000202	0680			157	BCTR R8, 0	Inititalize FIRST base register	
00000204	0680			158	BCTR R8, 0	Inititalize FIRST base register	
00000206	4190 8800		00000800	160	LA R9, 2048(, R8)	Inititalize SECOND base register	
0000020A	4190 9800		00000800	161	LA R9, 2048(, R9)	Inititalize SECOND base register	
				162			

[illegible]

[illegible]

LOC	OBJECT CODE		ADDR1	ADDR2	STMT				
					258	*****			
					259	*	RPERROR	Report instruction test in error	
					260	*****			
0000032C	50F0	8190		00000390	262	RPERROR	ST	R15, RPTSAVE	Save return address
00000330	5050	8194		00000394	263		ST	R5, RPTSVR5	Save R5
					264	*			
00000334	4820	5004		00000004	265		LH	R2, TNUM	get test number and convert
00000338	4E20	8E73		00001073	266		CVD	R2, DECNUM	
0000033C	D211	8E5D	8E47	0000105D	267		MVC	PRT3, EDIT	
00000342	DE11	8E5D	8E73	0000105D	268		ED	PRT3, DECNUM	
00000348	D202	8E18	8E6A	00001018	269		MVC	PRTNUM(3), PRT3+13	fill in message with test #
					270				
0000034E	D207	8E33	5008	00001033	271		MVC	PRTNAME, OPNAME	fill in message with instruction
					272	*			
00000354	E320	5007	0076	00000007	273		LB	R2, m4	get m4 and convert
0000035A	4E20	8E73		00001073	274		CVD	R2, DECNUM	
0000035E	D211	8E5D	8E47	0000105D	275		MVC	PRT3, EDIT	
00000364	DE11	8E5D	8E73	0000105D	276		ED	PRT3, DECNUM	
0000036A	D201	8E44	8E6B	00001044	277		MVC	PRTM4(2), PRT3+14	fill in message with m4 field
					278	*			
					279	*	Use Hercules Diagnose for Message to console		
					280	*			
00000370	9002	8198		00000398	281		STM	R0, R2, RPTDWSAV	save regs used by MSG
00000374	4100	003F		0000003F	282		LA	R0, PRTLNG	message length
00000378	4110	8E08		00001008	283		LA	R1, PRTLNE	messagfe address
0000037C	4520	81A8		000003A8	284		BAL	R2, MSG	call Hercules console MSG display
00000380	9802	8198		00000398	285		LM	R0, R2, RPTDWSAV	restore regs
00000384	5850	8194		00000394	287		L	R5, RPTSVR5	Restore R5
00000388	58F0	8190		00000390	288		L	R15, RPTSAVE	Restore return address
0000038C	07FF				289		BR	R15	Return to caller
00000390	00000000				291	RPTSAVE	DC	F' 0'	R15 save area
00000394	00000000				292	RPTSVR5	DC	F' 0'	R5 save area
00000398	00000000	00000000			294	RPTDWSAV	DC	2D' 0'	R0-R2 save area for MSG call

[illegible]

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				412	*****
				413	* E7TEST DSECT
				414	*****
				416	E7TEST DSECT ,
00000000	00000000			417	TSUB DC A(0) pointer to test
00000004	0000			418	TNUM DC H' 00' Test Number
00000006	00			419	DC X' 00'
00000007	00			420	M4 DC HL1' 00' m4 used
				421	
00000008	40404040	40404040		422	OPNAME DC CL8' ' E7 name
00000010	00000000			423	V2ADDR DC A(0) address of v2 source
00000014	00000000			424	V3ADDR DC A(0) address of v3 source
00000018	00000000			425	RELEN DC A(0) RESULT LENGTH
0000001C	00000000			426	READDR DC A(0) result (expected) address
00000020	00000000	00000000		427	DS FD gap
00000028	00000000	00000000		428	V10OUTPUT DS XL16 V1 Output
00000038	00000000	00000000		429	DS FD gap
				430	
				431	* test routine will be here (from VRR-c macro)
				432	*
				433	* followed by
				434	* EXPECTED RESULT
		00000000	00002B9F	436	ZVE7TST CSECT ,
000010B4				437	DS 0F
				439	*****
				440	* Macros to help build test tables
				441	*****
				443	*
				444	* macro to generate individual test
				445	*
				446	MACRO
				447	VRR_C &INST, &M4
				448	. * &INST - VRR-c instruction under test
				449	. * &m4 - m4 field
				450	
				451	GBLA &TNUM
				452	&TNUM SETA &TNUM+1
				453	
				454	DS 0FD
				455	USING *, R5 base for test data and test routine
				456	
				457	T&TNUM DC A(X&TNUM) address of test routine
				458	DC H' &TNUM test number
				459	DC X' 00'
				460	DC HL1' &M4' m4
				461	DC CL8' &INST' instruction name
				462	DC A(RE&TNUM+16) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				463	DC	A(RE&TNUM+32)	address of v3 source
				464	DC	A(16)	result length
				465	REA&TNUM	DC	A(RE&TNUM)
				466	DS	FD	gap
				467	V10&TNUM	DS	XL16
				468	DS	FD	gap
				469	. *		
				470	*		
				471	X&TNUM	DS	OF
				472	LGF	R1, V2ADDR	load v2 source
				473	VL	v22, 0(R1)	use v22 to test decoder
				474			
				475	LGF	R1, V3ADDR	load v3 source
				476	VL	v23, 0(R1)	use v23 to test decoder
				477			
				478	&INST	V22, V22, V23, &M4	test instruction (dest is a source)
				479	VST	V22, V10&TNUM	save v1 output
				480			
				481	BR	R11	return
				482			
				483	RE&TNUM	DC	OF
				484			xl16 expected result
				485	DROP	R5	
				486	MEND		
				488	*		
				489	*	macro to generate table of pointers to individual tests	
				490	*		
				491	MACRO		
				492	PTTABLE		
				493	GBLA	&TNUM	
				494	LCLA	&CUR	
				495	&CUR	SETA	1
				496	. *		
				497	TTABLE	DS	OF
				498	. LOOP	ANOP	
				499	. *		
				500	DC	A(T&CUR)	
				501	. *		
				502	&CUR	SETA	&CUR+1
				503	AIF	(&CUR LE &TNUM). LOOP	
				504	*		
				505	DC	A(0)	END OF TABLE
				506	DC	A(0)	
				507	. *		
				508	MEND		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				510	*****
				511	* E7 VRR-c tests
				512	*****
				513	PRINT DATA
				514	
				515	* E760 VMRL - Vector Merge Low
				516	* E761 VMRH - Vector Merge High
				517	* E794 VPK - Vector Pack
				518	*
				519	* VRR-c instruction, m4
				520	* followed by
				521	* 16 byte expected result (V1)
				522	* 16 byte V2 source
				523	* 16 byte V3 source
				524	*
				525	*-----
				526	* VMRL - Vector Merge Low
				527	*-----
				528	*Byte
				529	VRR_C VMRL, 0
000010B8				530+	DS OFD
000010B8		000010B8		531+	USING *, R5
000010B8	000010F8			532+T1	DC A(X1)
000010BC	0001			533+	DC H' 1'
000010BE	00			534+	DC X' 00'
000010BF	00			535+	DC HL1' 0'
000010C0	E5D4D9D3 40404040			536+	DC CL8' VMRL'
000010C8	00001130			537+	DC A(RE1+16)
000010CC	00001140			538+	DC A(RE1+32)
000010D0	00000010			539+	DC A(16)
000010D4	00001120			540+REA1	DC A(RE1)
000010D8	00000000 00000000			541+	DS FD
000010E0	00000000 00000000			542+V101	DS XL16
000010E8	00000000 00000000				
000010F0	00000000 00000000			543+	DS FD
				544+	*
000010F8				545+X1	DS OF
000010F8	E310 5010 0014		00000010	546+	LGF R1, V2ADDR
000010FE	E761 0000 0806		00000000	547+	VL v22, 0(R1)
00001104	E310 5014 0014		00000014	548+	LGF R1, V3ADDR
0000110A	E771 0000 0806		00000000	549+	VL v23, 0(R1)
00001110	E766 7000 0E60			550+	VMRL V22, V22, V23, 0
00001116	E760 5028 080E		000010E0	551+	VST V22, V101
0000111C	07FB			552+	BR R11
00001120				553+RE1	DC OF
00001120				554+	DROP R5
00001120	0109020A 030B040C			555	DC XL16' 0109020A030B040C 050D060E070F0800'
00001128	050D060E 070F0800				
00001130	FFFFFFFF FFFFFFFF			556	DC XL16' FFFFFFFFFFFFFFFFFF 0102030405060708'
00001138	01020304 05060708				
00001140	01020304 05060708			557	DC XL16' 0102030405060708 090A0B0C0D0E0F00'
00001148	090A0B0C 0D0E0F00				
				558	
				559	VRR_C VMRL, 0
00001150				560+	DS OFD
00001150		00001150		561+	USING *, R5

base for test data and test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001150	00001190			562+T2	DC	A(X2)	address of test routine
00001154	0002			563+	DC	H' 2'	test number
00001156	00			564+	DC	X' 00'	
00001157	00			565+	DC	HL1' 0'	m4
00001158	E5D4D9D3 40404040			566+	DC	CL8' VMRL'	instruction name
00001160	000011C8			567+	DC	A(RE2+16)	address of v2 source
00001164	000011D8			568+	DC	A(RE2+32)	address of v3 source
00001168	00000010			569+	DC	A(16)	result length
0000116C	000011B8			570+REA2	DC	A(RE2)	result address
00001170	00000000 00000000			571+	DS	FD	gap
00001178	00000000 00000000			572+V102	DS	XL16	V1 output
00001180	00000000 00000000						
00001188	00000000 00000000			573+	DS	FD	gap
				574+*			
00001190				575+X2	DS	OF	
00001190	E310 5010 0014		00000010	576+	LGF	R1, V2ADDR	load v2 source
00001196	E761 0000 0806		00000000	577+	VL	v22, 0(R1)	use v22 to test decoder
0000119C	E310 5014 0014		00000014	578+	LGF	R1, V3ADDR	load v3 source
000011A2	E771 0000 0806		00000000	579+	VL	v23, 0(R1)	use v23 to test decoder
000011A8	E766 7000 0E60			580+	VMRL	V22, V22, V23, 0	test instruction (dest is a source)
000011AE	E760 5028 080E		00001178	581+	VST	V22, V102	save v1 output
000011B4	07FB			582+	BR	R11	return
000011B8				583+RE2	DC	OF	xl16 expected result
000011B8				584+	DROP	R5	
000011B8	09010A02 0B030C04			585	DC	XL16' 09010A020B030C04 0D050E060F070008'	result t
000011C0	0D050E06 0F070008						
000011C8	FFFFFFFF FFFFFFFF			586	DC	XL16' FFFFFFFFFFFFFFFFFF 090A0B0C0D0E0F00'	v2
000011D0	090A0B0C 0D0E0F00						
000011D8	090A0B0C 0D0E0F00			587	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3
000011E0	01020304 05060708						
				588			
				589	VRR_C	VMRL, 0	
000011E8				590+	DS	OFD	
000011E8		000011E8		591+	USING	*, R5	base for test data and test routine
000011E8	00001228			592+T3	DC	A(X3)	address of test routine
000011EC	0003			593+	DC	H' 3'	test number
000011EE	00			594+	DC	X' 00'	
000011EF	00			595+	DC	HL1' 0'	m4
000011F0	E5D4D9D3 40404040			596+	DC	CL8' VMRL'	instruction name
000011F8	00001260			597+	DC	A(RE3+16)	address of v2 source
000011FC	00001270			598+	DC	A(RE3+32)	address of v3 source
00001200	00000010			599+	DC	A(16)	result length
00001204	00001250			600+REA3	DC	A(RE3)	result address
00001208	00000000 00000000			601+	DS	FD	gap
00001210	00000000 00000000			602+V103	DS	XL16	V1 output
00001218	00000000 00000000						
00001220	00000000 00000000			603+	DS	FD	gap
				604+*			
00001228				605+X3	DS	OF	
00001228	E310 5010 0014		00000010	606+	LGF	R1, V2ADDR	load v2 source
0000122E	E761 0000 0806		00000000	607+	VL	v22, 0(R1)	use v22 to test decoder
00001234	E310 5014 0014		00000014	608+	LGF	R1, V3ADDR	load v3 source
0000123A	E771 0000 0806		00000000	609+	VL	v23, 0(R1)	use v23 to test decoder
00001240	E766 7000 0E60			610+	VMRL	V22, V22, V23, 0	test instruction (dest is a source)
00001246	E760 9010 080E		00001210	611+	VST	V22, V103	save v1 output
0000124C	07FB			612+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001250				613+RE3	DC	0F	xl16 expected result
00001250				614+	DROP	R5	
00001250	09F10AF2 0BF30CF4			615	DC	XL16' 09F10AF20BF30CF4 0DF50EF60FF700F8'	result
00001258	0DF50EF6 0FF700F8						
00001260	FFFFFFFF FFFFFFFF			616	DC	XL16' FFFFFFFFFFFFFFFFFF 090A0B0C0D0E0F00'	v2
00001268	090A0B0C 0D0E0F00						
00001270	090A0B0C 0D0E0F00			617	DC	XL16' 090A0B0C0D0E0F00 F1F2F3F4F5F6F7F8'	v3
00001278	F1F2F3F4 F5F6F7F8						
				618			
00001280				619	VRR_C	VMRL, 0	
00001280		00001280		620+	DS	0FD	
00001280	000012C0			621+	USING	*, R5	base for test data and test routine
00001280	0004			622+T4	DC	A(X4)	address of test routine
00001284	00			623+	DC	H' 4'	test number
00001286	00			624+	DC	X' 00'	
00001287	00			625+	DC	HL1' 0'	m4
00001288	E5D4D9D3 40404040			626+	DC	CL8' VMRL'	instruction name
00001290	000012F8			627+	DC	A(RE4+16)	address of v2 source
00001294	00001308			628+	DC	A(RE4+32)	address of v3 source
00001298	00000010			629+	DC	A(16)	result length
0000129C	000012E8			630+REA4	DC	A(RE4)	result address
000012A0	00000000 00000000			631+	DS	FD	gap
000012A8	00000000 00000000			632+V104	DS	XL16	V1 output
000012B0	00000000 00000000						
000012B8	00000000 00000000			633+	DS	FD	gap
				634+*			
000012C0				635+X4	DS	0F	
000012C0	E310 5010 0014		00000010	636+	LGF	R1, V2ADDR	load v2 source
000012C6	E761 0000 0806		00000000	637+	VL	v22, 0(R1)	use v22 to test decoder
000012CC	E310 5014 0014		00000014	638+	LGF	R1, V3ADDR	load v3 source
000012D2	E771 0000 0806		00000000	639+	VL	v23, 0(R1)	use v23 to test decoder
000012D8	E766 7000 0E60			640+	VMRL	V22, V22, V23, 0	test instruction (dest is a source)
000012DE	E760 5028 080E		000012A8	641+	VST	V22, V104	save v1 output
000012E4	07FB			642+	BR	R11	return
000012E8				643+RE4	DC	0F	xl16 expected result
000012E8				644+	DROP	R5	
000012E8	F109F20A F30BF40C			645	DC	XL16' F109F20AF30BF40C F50DF60EF70FF800'	result
000012F0	F50DF60E F70FF800						
000012F8	FFFFFFFF FFFFFFFF			646	DC	XL16' FFFFFFFFFFFFFFFFFF F1F2F3F4F5F6F7F8'	v2
00001300	F1F2F3F4 F5F6F7F8						
00001308	01020304 05060708			647	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
00001310	090A0B0C 0D0E0F00						
				648			
				649 *Halfword			
				650	VRR_C	VMRL, 1	
00001318				651+	DS	0FD	
00001318		00001318		652+	USING	*, R5	base for test data and test routine
00001318	00001358			653+T5	DC	A(X5)	address of test routine
0000131C	0005			654+	DC	H' 5'	test number
0000131E	00			655+	DC	X' 00'	
0000131F	01			656+	DC	HL1' 1'	m4
00001320	E5D4D9D3 40404040			657+	DC	CL8' VMRL'	instruction name
00001328	00001390			658+	DC	A(RE5+16)	address of v2 source
0000132C	000013A0			659+	DC	A(RE5+32)	address of v3 source
00001330	00000010			660+	DC	A(16)	result length
00001334	00001380			661+REA5	DC	A(RE5)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001338	00000000	00000000		662+	DS	FD	gap	
00001340	00000000	00000000		663+V105	DS	XL16	V1 output	
00001348	00000000	00000000						
00001350	00000000	00000000		664+	DS	FD	gap	
				665+*				
00001358				666+X5	DS	OF		
00001358	E310 5010 0014		00000010	667+	LGF	R1, V2ADDR	load v2 source	
0000135E	E761 0000 0806		00000000	668+	VL	v22, 0(R1)	use v22 to test decoder	
00001364	E310 5014 0014		00000014	669+	LGF	R1, V3ADDR	load v3 source	
0000136A	E771 0000 0806		00000000	670+	VL	v23, 0(R1)	use v23 to test decoder	
00001370	E766 7000 1E60			671+	VMRL	V22, V22, V23, 1	test instruction (dest is a source)	
00001376	E760 5028 080E		00001340	672+	VST	V22, V105	save v1 output	
0000137C	07FB			673+	BR	R11	return	
00001380				674+RE5	DC	OF	xl16 expected result	
00001380				675+	DROP	R5		
00001380	0102090A 03040B0C			676	DC	XL16' 0102090A03040B0C 05060D0E07080F00'	result t	
00001388	05060D0E 07080F00							
00001390	FFFFFFFF FFFFFFFF			677	DC	XL16' FFFFFFFFFFFFFFFFFF 0102030405060708'	v2	
00001398	01020304 05060708							
000013A0	01020304 05060708			678	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3	
000013A8	090A0B0C 0D0E0F00							
				679				
000013B0				680	VRR_C	VMRL, 1		
000013B0		000013B0		681+	DS	OFD		
000013B0	000013F0			682+	USING	*, R5	base for test data and test routine	
000013B4	0006			683+T6	DC	A(X6)	address of test routine	
000013B6	00			684+	DC	H' 6'	test number	
000013B7	01			685+	DC	X' 00'		
000013B8	E5D4D9D3 40404040			686+	DC	HL1' 1'	m4	
000013C0	00001428			687+	DC	CL8' VMRL'	instruction name	
000013C4	00001438			688+	DC	A(RE6+16)	address of v2 source	
000013C8	00000010			689+	DC	A(RE6+32)	address of v3 source	
000013CC	00001418			690+	DC	A(16)	result length	
000013D0	00000000 00000000			691+REA6	DC	A(RE6)	result address	
000013D8	00000000 00000000			692+	DS	FD	gap	
000013E0	00000000 00000000			693+V106	DS	XL16	V1 output	
000013E8	00000000 00000000			694+	DS	FD	gap	
				695+*				
000013F0				696+X6	DS	OF		
000013F0	E310 5010 0014		00000010	697+	LGF	R1, V2ADDR	load v2 source	
000013F6	E761 0000 0806		00000000	698+	VL	v22, 0(R1)	use v22 to test decoder	
000013FC	E310 5014 0014		00000014	699+	LGF	R1, V3ADDR	load v3 source	
00001402	E771 0000 0806		00000000	700+	VL	v23, 0(R1)	use v23 to test decoder	
00001408	E766 7000 1E60			701+	VMRL	V22, V22, V23, 1	test instruction (dest is a source)	
0000140E	E760 5028 080E		000013D8	702+	VST	V22, V106	save v1 output	
00001414	07FB			703+	BR	R11	return	
00001418				704+RE6	DC	OF	xl16 expected result	
00001418				705+	DROP	R5		
00001418	090A0102 0B0C0304			706	DC	XL16' 090A01020B0C0304 0D0E05060F000708'	result t	
00001420	0D0E0506 0F000708							
00001428	FFFFFFFF FFFFFFFF			707	DC	XL16' FFFFFFFFFFFFFFFFFF 090A0B0C0D0E0F00'	v2	
00001430	090A0B0C 0D0E0F00							
00001438	090A0B0C 0D0E0F00			708	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3	
00001440	01020304 05060708							
				709				

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001448				710	VRR_C VMRL, 1		
00001448				711+	DS OFD		
00001448		00001448		712+	USING *, R5	base for test data and test routine	
00001448	00001488			713+T7	DC A(X7)	address of test routine	
0000144C	0007			714+	DC H' 7'	test number	
0000144E	00			715+	DC X' 00'		
0000144F	01			716+	DC HL1' 1'	m4	
00001450	E5D4D9D3 40404040			717+	DC CL8' VMRL'	instruction name	
00001458	000014C0			718+	DC A(RE7+16)	address of v2 source	
0000145C	000014D0			719+	DC A(RE7+32)	address of v3 source	
00001460	00000010			720+	DC A(16)	result length	
00001464	000014B0			721+REA7	DC A(RE7)	result address	
00001468	00000000 00000000			722+	DS FD	gap	
00001470	00000000 00000000			723+V107	DS XL16	V1 output	
00001478	00000000 00000000						
00001480	00000000 00000000			724+	DS FD	gap	
				725+*			
00001488				726+X7	DS OF		
00001488	E310 5010 0014		00000010	727+	LGF R1, V2ADDR	load v2 source	
0000148E	E761 0000 0806		00000000	728+	VL v22, 0(R1)	use v22 to test decoder	
00001494	E310 5014 0014		00000014	729+	LGF R1, V3ADDR	load v3 source	
0000149A	E771 0000 0806		00000000	730+	VL v23, 0(R1)	use v23 to test decoder	
000014A0	E766 7000 1E60			731+	VMRL V22, V22, V23, 1	test instruction (dest is a source)	
000014A6	E760 5028 080E		00001470	732+	VST V22, V107	save v1 output	
000014AC	07FB			733+	BR R11	return	
000014B0				734+RE7	DC OF	xl16 expected result	
000014B0				735+	DROP R5		
000014B0	090AF1F2 0B0CF3F4			736	DC XL16' 090AF1F20B0CF3F4 0D0EF5F60F00F7F8'	result t	
000014B8	0D0EF5F6 0F00F7F8						
000014C0	FFFFFFFF FFFFFFFF			737	DC XL16' FFFFFFFFFFFFFFFFFF 090A0B0C0D0E0F00'	v2	
000014C8	090A0B0C 0D0E0F00						
000014D0	090A0B0C 0D0E0F00			738	DC XL16' 090A0B0C0D0E0F00 F1F2F3F4F5F6F7F8'	v3	
000014D8	F1F2F3F4 F5F6F7F8						
				739			
000014E0				740	VRR_C VMRL, 1		
000014E0				741+	DS OFD		
000014E0		000014E0		742+	USING *, R5	base for test data and test routine	
000014E0	00001520			743+T8	DC A(X8)	address of test routine	
000014E4	0008			744+	DC H' 8'	test number	
000014E6	00			745+	DC X' 00'		
000014E7	01			746+	DC HL1' 1'	m4	
000014E8	E5D4D9D3 40404040			747+	DC CL8' VMRL'	instruction name	
000014F0	00001558			748+	DC A(RE8+16)	address of v2 source	
000014F4	00001568			749+	DC A(RE8+32)	address of v3 source	
000014F8	00000010			750+	DC A(16)	result length	
000014FC	00001548			751+REA8	DC A(RE8)	result address	
00001500	00000000 00000000			752+	DS FD	gap	
00001508	00000000 00000000			753+V108	DS XL16	V1 output	
00001510	00000000 00000000						
00001518	00000000 00000000			754+	DS FD	gap	
				755+*			
00001520				756+X8	DS OF		
00001520	E310 5010 0014		00000010	757+	LGF R1, V2ADDR	load v2 source	
00001526	E761 0000 0806		00000000	758+	VL v22, 0(R1)	use v22 to test decoder	
0000152C	E310 5014 0014		00000014	759+	LGF R1, V3ADDR	load v3 source	
00001532	E771 0000 0806		00000000	760+	VL v23, 0(R1)	use v23 to test decoder	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001538	E766 7000 1E60			761+	VMRL	V22, V22, V23, 1	test instruction (dest is a source)
0000153E	E760 5028 080E		00001508	762+	VST	V22, V108	save v1 output
00001544	07FB			763+	BR	R11	return
00001548				764+RE8	DC	0F	xl16 expected result
00001548				765+	DROP	R5	
00001548	F1F2090A F3F40B0C			766	DC	XL16' F1F2090AF3F40B0C F5F60D0EF7F80F00'	result t
00001550	F5F60D0E F7F80F00						
00001558	FFFFFFFF FFFFFFFF			767	DC	XL16' FFFFFFFFFFFFFFFFFF F1F2F3F4F5F6F7F8'	v2
00001560	F1F2F3F4 F5F6F7F8						
00001568	01020304 05060708			768	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
00001570	090A0B0C 0D0E0F00						
				769			
				770 *Word			
				771	VRR_C	VMRL, 2	
00001578				772+	DS	0FD	
00001578		00001578		773+	USING	*, R5	base for test data and test routine
00001578	000015B8			774+T9	DC	A(X9)	address of test routine
0000157C	0009			775+	DC	H' 9'	test number
0000157E	00			776+	DC	X' 00'	
0000157F	02			777+	DC	HL1' 2'	m4
00001580	E5D4D9D3 40404040			778+	DC	CL8' VMRL'	instruction name
00001588	000015F0			779+	DC	A(RE9+16)	address of v2 source
0000158C	00001600			780+	DC	A(RE9+32)	address of v3 source
00001590	00000010			781+	DC	A(16)	result length
00001594	000015E0			782+REA9	DC	A(RE9)	result address
00001598	00000000 00000000			783+	DS	FD	gap
000015A0	00000000 00000000			784+V109	DS	XL16	V1 output
000015A8	00000000 00000000						
000015B0	00000000 00000000			785+	DS	FD	gap
				786+*			
000015B8				787+X9	DS	0F	
000015B8	E310 5010 0014		00000010	788+	LGF	R1, V2ADDR	load v2 source
000015BE	E761 0000 0806		00000000	789+	VL	v22, 0(R1)	use v22 to test decoder
000015C4	E310 5014 0014		00000014	790+	LGF	R1, V3ADDR	load v3 source
000015CA	E771 0000 0806		00000000	791+	VL	v23, 0(R1)	use v23 to test decoder
000015D0	E766 7000 2E60			792+	VMRL	V22, V22, V23, 2	test instruction (dest is a source)
000015D6	E760 5028 080E		000015A0	793+	VST	V22, V109	save v1 output
000015DC	07FB			794+	BR	R11	return
000015E0				795+RE9	DC	0F	xl16 expected result
000015E0				796+	DROP	R5	
000015E0	01020304 090A0B0C			797	DC	XL16' 01020304090A0B0C 050607080D0E0F00'	result t
000015E8	05060708 0D0E0F00						
000015F0	FFFFFFFF FFFFFFFF			798	DC	XL16' FFFFFFFFFFFFFFFFFF 0102030405060708'	v2
000015F8	01020304 05060708						
00001600	01020304 05060708			799	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
00001608	090A0B0C 0D0E0F00						
				800			
				801	VRR_C	VMRL, 2	
00001610				802+	DS	0FD	
00001610		00001610		803+	USING	*, R5	base for test data and test routine
00001610	00001650			804+T10	DC	A(X10)	address of test routine
00001614	000A			805+	DC	H' 10'	test number
00001616	00			806+	DC	X' 00'	
00001617	02			807+	DC	HL1' 2'	m4
00001618	E5D4D9D3 40404040			808+	DC	CL8' VMRL'	instruction name
00001620	00001688			809+	DC	A(RE10+16)	address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001624	00001698			810+	DC	A(RE10+32)	address of v3 source
00001628	00000010			811+	DC	A(16)	result length
0000162C	00001678			812+REA10	DC	A(RE10)	result address
00001630	00000000 00000000			813+	DS	FD	gap
00001638	00000000 00000000			814+V1010	DS	XL16	V1 output
00001640	00000000 00000000						
00001648	00000000 00000000			815+	DS	FD	gap
				816+*			
00001650				817+X10	DS	0F	
00001650	E310 5010 0014		00000010	818+	LGF	R1, V2ADDR	load v2 source
00001656	E761 0000 0806		00000000	819+	VL	v22, 0(R1)	use v22 to test decoder
0000165C	E310 5014 0014		00000014	820+	LGF	R1, V3ADDR	load v3 source
00001662	E771 0000 0806		00000000	821+	VL	v23, 0(R1)	use v23 to test decoder
00001668	E766 7000 2E60			822+	VMRL	V22, V22, V23, 2	test instruction (dest is a source)
0000166E	E760 5028 080E		00001638	823+	VST	V22, V1010	save v1 output
00001674	07FB			824+	BR	R11	return
00001678				825+RE10	DC	0F	xl16 expected result
00001678				826+	DROP	R5	
00001678	090A0B0C 01020304			827	DC	XL16' 090A0B0C01020304 0D0E0F0005060708'	result t
00001680	0D0E0F00 05060708						
00001688	FFFFFFFF FFFFFFFF			828	DC	XL16' FFFFFFFFFFFFFFFFFF 090A0B0C0D0E0F00'	v2
00001690	090A0B0C 0D0E0F00						
00001698	090A0B0C 0D0E0F00			829	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3
000016A0	01020304 05060708						
				830			
000016A8				831	VRR_C	VMRL, 2	
000016A8		000016A8		832+	DS	0FD	
000016A8	000016E8			833+	USING	*, R5	base for test data and test routine
000016AC	000B			834+T11	DC	A(X11)	address of test routine
000016AE	00			835+	DC	H' 11'	test number
000016AF	02			836+	DC	X' 00'	
000016B0	E5D4D9D3 40404040			837+	DC	HL1' 2'	m4
000016B8	00001720			838+	DC	CL8' VMRL'	instruction name
000016BC	00001730			839+	DC	A(RE11+16)	address of v2 source
000016C0	00000010			840+	DC	A(RE11+32)	address of v3 source
000016C4	00001710			841+	DC	A(16)	result length
000016C8	00000000 00000000			842+REA11	DC	A(RE11)	result address
000016D0	00000000 00000000			843+	DS	FD	gap
000016D8	00000000 00000000			844+V1011	DS	XL16	V1 output
000016E0	00000000 00000000						
				845+	DS	FD	gap
				846+*			
000016E8				847+X11	DS	0F	
000016E8	E310 5010 0014		00000010	848+	LGF	R1, V2ADDR	load v2 source
000016EE	E761 0000 0806		00000000	849+	VL	v22, 0(R1)	use v22 to test decoder
000016F4	E310 5014 0014		00000014	850+	LGF	R1, V3ADDR	load v3 source
000016FA	E771 0000 0806		00000000	851+	VL	v23, 0(R1)	use v23 to test decoder
00001700	E766 7000 2E60			852+	VMRL	V22, V22, V23, 2	test instruction (dest is a source)
00001706	E760 5028 080E		000016D0	853+	VST	V22, V1011	save v1 output
0000170C	07FB			854+	BR	R11	return
00001710				855+RE11	DC	0F	xl16 expected result
00001710				856+	DROP	R5	
00001710	090A0B0C F1F2F3F4			857	DC	XL16' 090A0B0CF1F2F3F4 0D0E0F00F5F6F7F8'	result t
00001718	0D0E0F00 F5F6F7F8						
00001720	FFFFFFFF FFFFFFFF			858	DC	XL16' FFFFFFFFFFFFFFFFFF 090A0B0C0D0E0F00'	v2
00001728	090A0B0C 0D0E0F00						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001730	090A0B0C 0D0E0F00			859	DC	XL16' 090A0B0C0D0E0F00 F1F2F3F4F5F6F7F8'	v3
00001738	F1F2F3F4 F5F6F7F8						
				860			
				861	VRR_C	VMRL, 2	
00001740				862+	DS	0FD	
00001740		00001740		863+	USING	*, R5	base for test data and test routine
00001740	00001780			864+T12	DC	A(X12)	address of test routine
00001744	000C			865+	DC	H' 12'	test number
00001746	00			866+	DC	X' 00'	
00001747	02			867+	DC	HL1' 2'	m4
00001748	E5D4D9D3 40404040			868+	DC	CL8' VMRL'	instruction name
00001750	000017B8			869+	DC	A(RE12+16)	address of v2 source
00001754	000017C8			870+	DC	A(RE12+32)	address of v3 source
00001758	00000010			871+	DC	A(16)	result length
0000175C	000017A8			872+REA12	DC	A(RE12)	result address
00001760	00000000 00000000			873+	DS	FD	gap
00001768	00000000 00000000			874+V1012	DS	XL16	V1 output
00001770	00000000 00000000						
00001778	00000000 00000000			875+	DS	FD	gap
				876+*			
00001780				877+X12	DS	0F	
00001780	E310 5010 0014		00000010	878+	LGF	R1, V2ADDR	load v2 source
00001786	E761 0000 0806		00000000	879+	VL	v22, 0(R1)	use v22 to test decoder
0000178C	E310 5014 0014		00000014	880+	LGF	R1, V3ADDR	load v3 source
00001792	E771 0000 0806		00000000	881+	VL	v23, 0(R1)	use v23 to test decoder
00001798	E766 7000 2E60			882+	VMRL	V22, V22, V23, 2	test instruction (dest is a source)
0000179E	E760 5028 080E		00001768	883+	VST	V22, V1012	save v1 output
000017A4	07FB			884+	BR	R11	return
000017A8				885+RE12	DC	0F	xl16 expected result
000017A8				886+	DROP	R5	
000017A8	F1F2F3F4 090A0B0C			887	DC	XL16' F1F2F3F4090A0B0C F5F6F7F80D0E0F00'	result t
000017B0	F5F6F7F8 0D0E0F00						
000017B8	FFFFFFFF FFFFFFFF			888	DC	XL16' FFFFFFFFFFFFFFFFFF F1F2F3F4F5F6F7F8'	v2
000017C0	F1F2F3F4 F5F6F7F8						
000017C8	01020304 05060708			889	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
000017D0	090A0B0C 0D0E0F00						
				890			
				891	*Doubleword		
				892	VRR_C	VMRL, 3	
000017D8				893+	DS	0FD	
000017D8		000017D8		894+	USING	*, R5	base for test data and test routine
000017D8	00001818			895+T13	DC	A(X13)	address of test routine
000017DC	000D			896+	DC	H' 13'	test number
000017DE	00			897+	DC	X' 00'	
000017DF	03			898+	DC	HL1' 3'	m4
000017E0	E5D4D9D3 40404040			899+	DC	CL8' VMRL'	instruction name
000017E8	00001850			900+	DC	A(RE13+16)	address of v2 source
000017EC	00001860			901+	DC	A(RE13+32)	address of v3 source
000017F0	00000010			902+	DC	A(16)	result length
000017F4	00001840			903+REA13	DC	A(RE13)	result address
000017F8	00000000 00000000			904+	DS	FD	gap
00001800	00000000 00000000			905+V1013	DS	XL16	V1 output
00001808	00000000 00000000						
00001810	00000000 00000000			906+	DS	FD	gap
				907+*			
00001818				908+X13	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001818	E310 5010 0014		00000010	909+	LGF	R1, V2ADDR	load v2 source	
0000181E	E761 0000 0806		00000000	910+	VL	v22, 0(R1)	use v22 to test decoder	
00001824	E310 5014 0014		00000014	911+	LGF	R1, V3ADDR	load v3 source	
0000182A	E771 0000 0806		00000000	912+	VL	v23, 0(R1)	use v23 to test decoder	
00001830	E766 7000 3E60			913+	VMRL	V22, V22, V23, 3	test instruction (dest is a source)	
00001836	E760 5028 080E		00001800	914+	VST	V22, V1013	save v1 output	
0000183C	07FB			915+	BR	R11	return	
00001840				916+RE13	DC	0F	xl16 expected result	
00001840				917+	DROP	R5		
00001840	01020304 05060708			918	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	result t	
00001848	090A0B0C 0D0E0F00							
00001850	FFFFFFFF FFFFFFFF			919	DC	XL16' FFFFFFFFFFFFFFFFFF 0102030405060708'	v2	
00001858	01020304 05060708							
00001860	01020304 05060708			920	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3	
00001868	090A0B0C 0D0E0F00							
				921				
				922	VRR_C	VMRL, 3		
00001870				923+	DS	0FD		
00001870		00001870		924+	USING	*, R5	base for test data and test routine	
00001870	000018B0			925+T14	DC	A(X14)	address of test routine	
00001874	000E			926+	DC	H' 14'	test number	
00001876	00			927+	DC	X' 00'		
00001877	03			928+	DC	HL1' 3'	m4	
00001878	E5D4D9D3 40404040			929+	DC	CL8' VMRL'	instruction name	
00001880	000018E8			930+	DC	A(RE14+16)	address of v2 source	
00001884	000018F8			931+	DC	A(RE14+32)	address of v3 source	
00001888	00000010			932+	DC	A(16)	result length	
0000188C	000018D8			933+REA14	DC	A(RE14)	result address	
00001890	00000000 00000000			934+	DS	FD	gap	
00001898	00000000 00000000			935+V1014	DS	XL16	V1 output	
000018A0	00000000 00000000							
000018A8	00000000 00000000			936+	DS	FD	gap	
				937+*				
000018B0				938+X14	DS	0F		
000018B0	E310 5010 0014		00000010	939+	LGF	R1, V2ADDR	load v2 source	
000018B6	E761 0000 0806		00000000	940+	VL	v22, 0(R1)	use v22 to test decoder	
000018BC	E310 5014 0014		00000014	941+	LGF	R1, V3ADDR	load v3 source	
000018C2	E771 0000 0806		00000000	942+	VL	v23, 0(R1)	use v23 to test decoder	
000018C8	E766 7000 3E60			943+	VMRL	V22, V22, V23, 3	test instruction (dest is a source)	
000018CE	E760 5028 080E		00001898	944+	VST	V22, V1014	save v1 output	
000018D4	07FB			945+	BR	R11	return	
000018D8				946+RE14	DC	0F	xl16 expected result	
000018D8				947+	DROP	R5		
000018D8	090A0B0C 0D0E0F00			948	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	result t	
000018E0	01020304 05060708							
000018E8	FFFFFFFF FFFFFFFF			949	DC	XL16' FFFFFFFFFFFFFFFFFF 090A0B0C0D0E0F00'	v2	
000018F0	090A0B0C 0D0E0F00							
000018F8	090A0B0C 0D0E0F00			950	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3	
00001900	01020304 05060708							
				951				
				952	VRR_C	VMRL, 3		
00001908				953+	DS	0FD		
00001908		00001908		954+	USING	*, R5	base for test data and test routine	
00001908	00001948			955+T15	DC	A(X15)	address of test routine	
0000190C	000F			956+	DC	H' 15'	test number	
0000190E	00			957+	DC	X' 00'		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000190F	03			958+	DC	HL1' 3'	m4
00001910	E5D4D9D3 40404040			959+	DC	CL8' VMRL'	instruction name
00001918	00001980			960+	DC	A(RE15+16)	address of v2 source
0000191C	00001990			961+	DC	A(RE15+32)	address of v3 source
00001920	00000010			962+	DC	A(16)	result length
00001924	00001970			963+REA15	DC	A(RE15)	result address
00001928	00000000 00000000			964+	DS	FD	gap
00001930	00000000 00000000			965+V1015	DS	XL16	V1 output
00001938	00000000 00000000						
00001940	00000000 00000000			966+	DS	FD	gap
				967+*			
00001948				968+X15	DS	0F	
00001948	E310 5010 0014		00000010	969+	LGF	R1, V2ADDR	load v2 source
0000194E	E761 0000 0806		00000000	970+	VL	v22, 0(R1)	use v22 to test decoder
00001954	E310 5014 0014		00000014	971+	LGF	R1, V3ADDR	load v3 source
0000195A	E771 0000 0806		00000000	972+	VL	v23, 0(R1)	use v23 to test decoder
00001960	E766 7000 3E60			973+	VMRL	V22, V22, V23, 3	test instruction (dest is a source)
00001966	E760 5028 080E		00001930	974+	VST	V22, V1015	save v1 output
0000196C	07FB			975+	BR	R11	return
00001970				976+RE15	DC	0F	xl16 expected result
00001970				977+	DROP	R5	
00001970	090A0B0C 0D0E0F00			978	DC	XL16' 090A0B0C0D0E0F00 F1F2F3F4F5F6F7F8'	result t
00001978	F1F2F3F4 F5F6F7F8						
00001980	FFFFFFFF FFFFFFFF			979	DC	XL16' FFFFFFFFFFFFFFFFFF 090A0B0C0D0E0F00'	v2
00001988	090A0B0C 0D0E0F00						
00001990	090A0B0C 0D0E0F00			980	DC	XL16' 090A0B0C0D0E0F00 F1F2F3F4F5F6F7F8'	v3
00001998	F1F2F3F4 F5F6F7F8						
				981			
				982	VRR_C	VMRL, 3	
000019A0				983+	DS	0FD	
000019A0		000019A0		984+	USING	*, R5	base for test data and test routine
000019A0	000019E0			985+T16	DC	A(X16)	address of test routine
000019A4	0010			986+	DC	H' 16'	test number
000019A6	00			987+	DC	X' 00'	
000019A7	03			988+	DC	HL1' 3'	m4
000019A8	E5D4D9D3 40404040			989+	DC	CL8' VMRL'	instruction name
000019B0	00001A18			990+	DC	A(RE16+16)	address of v2 source
000019B4	00001A28			991+	DC	A(RE16+32)	address of v3 source
000019B8	00000010			992+	DC	A(16)	result length
000019BC	00001A08			993+REA16	DC	A(RE16)	result address
000019C0	00000000 00000000			994+	DS	FD	gap
000019C8	00000000 00000000			995+V1016	DS	XL16	V1 output
000019D0	00000000 00000000						
000019D8	00000000 00000000			996+	DS	FD	gap
				997+*			
				998+X16	DS	0F	
000019E0				999+	LGF	R1, V2ADDR	load v2 source
000019E0	E310 5010 0014		00000010	1000+	VL	v22, 0(R1)	use v22 to test decoder
000019E6	E761 0000 0806		00000000	1001+	LGF	R1, V3ADDR	load v3 source
000019EC	E310 5014 0014		00000014	1002+	VL	v23, 0(R1)	use v23 to test decoder
000019F2	E771 0000 0806		00000000	1003+	VMRL	V22, V22, V23, 3	test instruction (dest is a source)
000019F8	E766 7000 3E60			1004+	VST	V22, V1016	save v1 output
000019FE	E760 5028 080E		000019C8	1005+	BR	R11	return
00001A04	07FB			1006+RE16	DC	0F	xl16 expected result
00001A08				1007+	DROP	R5	
00001A08				1008	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	result t
00001A08	F1F2F3F4 F5F6F7F8						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001A10	090A0B0C 0D0E0F00						
00001A18	FFFFFFFF FFFFFFFF			1009	DC	XL16' FFFFFFFFFFFFFFFFFF F1F2F3F4F5F6F7F8'	v2
00001A20	F1F2F3F4 F5F6F7F8						
00001A28	01020304 05060708			1010	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
00001A30	090A0B0C 0D0E0F00						
				1011			
				1012	*-----		
				1013	* VMRH - Vector Merge High		
				1014	*-----		
				1015	*Byte		
				1016	VRR_C VMRH, 0		
00001A38				1017+	DS OFD		
00001A38		00001A38		1018+	USING *, R5	base for test data and test routine	
00001A38	00001A78			1019+T17	DC A(X17)	address of test routine	
00001A3C	0011			1020+	DC H' 17'	test number	
00001A3E	00			1021+	DC X' 00'		
00001A3F	00			1022+	DC HL1' 0'	m4	
00001A40	E5D4D9C8 40404040			1023+	DC CL8' VMRH'	instruction name	
00001A48	00001AB0			1024+	DC A(RE17+16)	address of v2 source	
00001A4C	00001AC0			1025+	DC A(RE17+32)	address of v3 source	
00001A50	00000010			1026+	DC A(16)	result length	
00001A54	00001AA0			1027+REA17	DC A(RE17)	result address	
00001A58	00000000 00000000			1028+	DS FD	gap	
00001A60	00000000 00000000			1029+V1017	DS XL16	V1 output	
00001A68	00000000 00000000						
00001A70	00000000 00000000			1030+	DS FD	gap	
				1031+*			
00001A78				1032+X17	DS OF		
00001A78	E310 5010 0014		00000010	1033+	LGF R1, V2ADDR	load v2 source	
00001A7E	E761 0000 0806		00000000	1034+	VL v22, 0(R1)	use v22 to test decoder	
00001A84	E310 5014 0014		00000014	1035+	LGF R1, V3ADDR	load v3 source	
00001A8A	E771 0000 0806		00000000	1036+	VL v23, 0(R1)	use v23 to test decoder	
00001A90	E766 7000 0E61			1037+	VMRH V22, V22, V23, 0	test instruction (dest is a source)	
00001A96	E760 5028 080E		00001A60	1038+	VST V22, V1017	save v1 output	
00001A9C	07FB			1039+	BR R11	return	
00001AA0				1040+RE17	DC OF	xl16 expected result	
00001AA0				1041+	DROP R5		
00001AA0	09010A02 0B030C04			1042	DC XL16' 09010A020B030C04 0D050E060F070008'	result t	
00001AA8	0D050E06 0F070008						
00001AB0	090A0B0C 0D0E0F00			1043	DC XL16' 090A0B0C0D0E0F00 FFFFFFFFFFFFFFFFFF'	v2	
00001AB8	FFFFFFFF FFFFFFFF						
00001AC0	01020304 05060708			1044	DC XL16' 0102030405060708 090A0B0C0D0E0F00'	v3	
00001AC8	090A0B0C 0D0E0F00						
				1045			
				1046	VRR_C VMRH, 0		
00001AD0				1047+	DS OFD		
00001AD0		00001AD0		1048+	USING *, R5	base for test data and test routine	
00001AD0	00001B10			1049+T18	DC A(X18)	address of test routine	
00001AD4	0012			1050+	DC H' 18'	test number	
00001AD6	00			1051+	DC X' 00'		
00001AD7	00			1052+	DC HL1' 0'	m4	
00001AD8	E5D4D9C8 40404040			1053+	DC CL8' VMRH'	instruction name	
00001AE0	00001B48			1054+	DC A(RE18+16)	address of v2 source	
00001AE4	00001B58			1055+	DC A(RE18+32)	address of v3 source	
00001AE8	00000010			1056+	DC A(16)	result length	
00001AEC	00001B38			1057+REA18	DC A(RE18)	result address	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001AF0	00000000 00000000			1058+	DS	FD	gap	
00001AF8	00000000 00000000			1059+V1018	DS	XL16	V1 output	
00001B00	00000000 00000000							
00001B08	00000000 00000000			1060+	DS	FD	gap	
				1061+*				
00001B10				1062+X18	DS	OF		
00001B10	E310 5010 0014		00000010	1063+	LGF	R1, V2ADDR	load v2 source	
00001B16	E761 0000 0806		00000000	1064+	VL	v22, 0(R1)	use v22 to test decoder	
00001B1C	E310 5014 0014		00000014	1065+	LGF	R1, V3ADDR	load v3 source	
00001B22	E771 0000 0806		00000000	1066+	VL	v23, 0(R1)	use v23 to test decoder	
00001B28	E766 7000 0E61			1067+	VMRH	V22, V22, V23, 0	test instruction (dest is a source)	
00001B2E	E760 5028 080E		00001AF8	1068+	VST	V22, V1018	save v1 output	
00001B34	07FB			1069+	BR	R11	return	
00001B38				1070+RE18	DC	OF	xl16 expected result	
00001B38				1071+	DROP	R5		
00001B38	0109020A 030B040C			1072	DC	XL16' 0109020A030B040C 050D060E070F0800'	result t	
00001B40	050D060E 070F0800							
00001B48	01020304 05060708			1073	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2	
00001B50	FFFFFFFF FFFFFFFF							
00001B58	090A0B0C 0D0E0F00			1074	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3	
00001B60	01020304 05060708							
				1075				
00001B68				1076	VRR_C	VMRH, 0		
00001B68		00001B68		1077+	DS	OFD		
00001B68	00001BA8			1078+	USING	*, R5	base for test data and test routine	
00001B6C	0013			1079+T19	DC	A(X19)	address of test routine	
00001B6E	00			1080+	DC	H' 19'	test number	
00001B6F	00			1081+	DC	X' 00'		
				1082+	DC	HL1' 0'	m4	
00001B70	E5D4D9C8 40404040			1083+	DC	CL8' VMRH'	instruction name	
00001B78	00001BE0			1084+	DC	A(RE19+16)	address of v2 source	
00001B7C	00001BF0			1085+	DC	A(RE19+32)	address of v3 source	
00001B80	00000010			1086+	DC	A(16)	result length	
00001B84	00001BD0			1087+REA19	DC	A(RE19)	result address	
00001B88	00000000 00000000			1088+	DS	FD	gap	
00001B90	00000000 00000000			1089+V1019	DS	XL16	V1 output	
00001B98	00000000 00000000							
00001BA0	00000000 00000000			1090+	DS	FD	gap	
				1091+*				
00001BA8				1092+X19	DS	OF		
00001BA8	E310 5010 0014		00000010	1093+	LGF	R1, V2ADDR	load v2 source	
00001BAE	E761 0000 0806		00000000	1094+	VL	v22, 0(R1)	use v22 to test decoder	
00001BB4	E310 5014 0014		00000014	1095+	LGF	R1, V3ADDR	load v3 source	
00001BBA	E771 0000 0806		00000000	1096+	VL	v23, 0(R1)	use v23 to test decoder	
00001BC0	E766 7000 0E61			1097+	VMRH	V22, V22, V23, 0	test instruction (dest is a source)	
00001BC6	E760 5028 080E		00001B90	1098+	VST	V22, V1019	save v1 output	
00001BCC	07FB			1099+	BR	R11	return	
00001BD0				1100+RE19	DC	OF	xl16 expected result	
00001BD0				1101+	DROP	R5		
00001BD0	01F102F2 03F304F4			1102	DC	XL16' 01F102F203F304F4 05F506F607F708F8'	result t	
00001BD8	05F506F6 07F708F8							
00001BE0	01020304 05060708			1103	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2	
00001BE8	FFFFFFFF FFFFFFFF							
00001BF0	F1F2F3F4 F5F6F7F8			1104	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v3	
00001BF8	090A0B0C 0D0E0F00							
				1105				

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001C00				1106	VRR_C VMRH, 0		
00001C00				1107+	DS OFD		
00001C00		00001C00		1108+	USING *, R5	base for test data and test routine	
00001C00	00001C40			1109+T20	DC A(X20)	address of test routine	
00001C04	0014			1110+	DC H' 20'	test number	
00001C06	00			1111+	DC X' 00'		
00001C07	00			1112+	DC HL1' 0'	m4	
00001C08	E5D4D9C8 40404040			1113+	DC CL8' VMRH'	instruction name	
00001C10	00001C78			1114+	DC A(RE20+16)	address of v2 source	
00001C14	00001C88			1115+	DC A(RE20+32)	address of v3 source	
00001C18	00000010			1116+	DC A(16)	result length	
00001C1C	00001C68			1117+REA20	DC A(RE20)	result address	
00001C20	00000000 00000000			1118+	DS FD	gap	
00001C28	00000000 00000000			1119+V1020	DS XL16	V1 output	
00001C30	00000000 00000000						
00001C38	00000000 00000000			1120+	DS FD	gap	
				1121+*			
00001C40				1122+X20	DS OF		
00001C40	E310 5010 0014		00000010	1123+	LGF R1, V2ADDR	load v2 source	
00001C46	E761 0000 0806		00000000	1124+	VL v22, 0(R1)	use v22 to test decoder	
00001C4C	E310 5014 0014		00000014	1125+	LGF R1, V3ADDR	load v3 source	
00001C52	E771 0000 0806		00000000	1126+	VL v23, 0(R1)	use v23 to test decoder	
00001C58	E766 7000 0E61			1127+	VMRH V22, V22, V23, 0	test instruction (dest is a source)	
00001C5E	E760 5028 080E		00001C28	1128+	VST V22, V1020	save v1 output	
00001C64	07FB			1129+	BR R11	return	
00001C68				1130+RE20	DC OF	xl16 expected result	
00001C68				1131+	DROP R5		
00001C68	F101F202 F303F404			1132	DC XL16' F101F202F303F404 F505F606F707F808'	result t	
00001C70	F505F606 F707F808						
00001C78	F1F2F3F4 F5F6F7F8			1133	DC XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v2	
00001C80	090A0B0C 0D0E0F00						
00001C88	01020304 05060708			1134	DC XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v3	
00001C90	FFFFFFFF FFFFFFFF						
				1135			
				1136 *Hal fword			
00001C98				1137	VRR_C VMRH, 1		
00001C98		00001C98		1138+	DS OFD		
00001C98	00001CD8			1139+	USING *, R5	base for test data and test routine	
00001C9C	0015			1140+T21	DC A(X21)	address of test routine	
00001C9E	00			1141+	DC H' 21'	test number	
00001C9F	01			1142+	DC X' 00'		
00001CA0	E5D4D9C8 40404040			1143+	DC HL1' 1'	m4	
00001CA8	00001D10			1144+	DC CL8' VMRH'	instruction name	
00001CAC	00001D20			1145+	DC A(RE21+16)	address of v2 source	
00001CB0	00000010			1146+	DC A(RE21+32)	address of v3 source	
00001CB4	00001D00			1147+	DC A(16)	result length	
00001CB8	00000000 00000000			1148+REA21	DC A(RE21)	result address	
00001CC0	00000000 00000000			1149+	DS FD	gap	
00001CC8	00000000 00000000			1150+V1021	DS XL16	V1 output	
00001CD0	00000000 00000000			1151+	DS FD	gap	
				1152+*			
00001CD8				1153+X21	DS OF		
00001CD8	E310 5010 0014		00000010	1154+	LGF R1, V2ADDR	load v2 source	
00001CDE	E761 0000 0806		00000000	1155+	VL v22, 0(R1)	use v22 to test decoder	
00001CE4	E310 5014 0014		00000014	1156+	LGF R1, V3ADDR	load v3 source	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001CEA	E771 0000 0806		00000000	1157+	VL	v23, 0(R1)	use v23 to test decoder
00001CF0	E766 7000 1E61			1158+	VMRH	V22, V22, V23, 1	test instruction (dest is a source)
00001CF6	E760 5028 080E		00001CC0	1159+	VST	V22, V1021	save v1 output
00001CFC	07FB			1160+	BR	R11	return
00001D00				1161+RE21	DC	0F	xl16 expected result
00001D00				1162+	DROP	R5	
00001D00	090A0102 0B0C0304			1163	DC	XL16' 090A01020B0C0304 0D0E05060F000708'	result t
00001D08	0D0E0506 0F000708						
00001D10	090A0B0C 0D0E0F00			1164	DC	XL16' 090A0B0C0D0E0F00 FFFFFFFFFFFFFFFFFF'	v2
00001D18	FFFFFFFF FFFFFFFF						
00001D20	01020304 05060708			1165	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
00001D28	090A0B0C 0D0E0F00						
				1166			
				1167	VRR_C	VMRH, 1	
00001D30				1168+	DS	0FD	
00001D30		00001D30		1169+	USING	*, R5	base for test data and test routine
00001D30	00001D70			1170+T22	DC	A(X22)	address of test routine
00001D34	0016			1171+	DC	H' 22'	test number
00001D36	00			1172+	DC	X' 00'	
00001D37	01			1173+	DC	HL1' 1'	m4
00001D38	E5D4D9C8 40404040			1174+	DC	CL8' VMRH'	instruction name
00001D40	00001DA8			1175+	DC	A(RE22+16)	address of v2 source
00001D44	00001DB8			1176+	DC	A(RE22+32)	address of v3 source
00001D48	00000010			1177+	DC	A(16)	result length
00001D4C	00001D98			1178+REA22	DC	A(RE22)	result address
00001D50	00000000 00000000			1179+	DS	FD	gap
00001D58	00000000 00000000			1180+V1022	DS	XL16	V1 output
00001D60	00000000 00000000						
00001D68	00000000 00000000			1181+	DS	FD	gap
				1182+*			
00001D70				1183+X22	DS	0F	
00001D70	E310 5010 0014		00000010	1184+	LGF	R1, V2ADDR	load v2 source
00001D76	E761 0000 0806		00000000	1185+	VL	v22, 0(R1)	use v22 to test decoder
00001D7C	E310 5014 0014		00000014	1186+	LGF	R1, V3ADDR	load v3 source
00001D82	E771 0000 0806		00000000	1187+	VL	v23, 0(R1)	use v23 to test decoder
00001D88	E766 7000 1E61			1188+	VMRH	V22, V22, V23, 1	test instruction (dest is a source)
00001D8E	E760 5028 080E		00001D58	1189+	VST	V22, V1022	save v1 output
00001D94	07FB			1190+	BR	R11	return
00001D98				1191+RE22	DC	0F	xl16 expected result
00001D98				1192+	DROP	R5	
00001D98	0102090A 03040B0C			1193	DC	XL16' 0102090A03040B0C 05060D0E07080F00'	result t
00001DA0	05060D0E 07080F00						
00001DA8	01020304 05060708			1194	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2
00001DB0	FFFFFFFF FFFFFFFF						
00001DB8	090A0B0C 0D0E0F00			1195	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3
00001DC0	01020304 05060708						
				1196			
				1197	VRR_C	VMRH, 1	
00001DC8				1198+	DS	0FD	
00001DC8		00001DC8		1199+	USING	*, R5	base for test data and test routine
00001DC8	00001E08			1200+T23	DC	A(X23)	address of test routine
00001DCC	0017			1201+	DC	H' 23'	test number
00001DCE	00			1202+	DC	X' 00'	
00001DCF	01			1203+	DC	HL1' 1'	m4
00001DD0	E5D4D9C8 40404040			1204+	DC	CL8' VMRH'	instruction name
00001DD8	00001E40			1205+	DC	A(RE23+16)	address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001DDC	00001E50			1206+	DC	A(RE23+32)	address of v3 source
00001DE0	00000010			1207+	DC	A(16)	result length
00001DE4	00001E30			1208+REA23	DC	A(RE23)	result address
00001DE8	00000000 00000000			1209+	DS	FD	gap
00001DF0	00000000 00000000			1210+V1023	DS	XL16	V1 output
00001DF8	00000000 00000000						
00001E00	00000000 00000000			1211+	DS	FD	gap
				1212+*			
00001E08				1213+X23	DS	0F	
00001E08	E310 5010 0014		00000010	1214+	LGF	R1, V2ADDR	load v2 source
00001E0E	E761 0000 0806		00000000	1215+	VL	v22, 0(R1)	use v22 to test decoder
00001E14	E310 5014 0014		00000014	1216+	LGF	R1, V3ADDR	load v3 source
00001E1A	E771 0000 0806		00000000	1217+	VL	v23, 0(R1)	use v23 to test decoder
00001E20	E766 7000 1E61			1218+	VMRH	V22, V22, V23, 1	test instruction (dest is a source)
00001E26	E760 5028 080E		00001DF0	1219+	VST	V22, V1023	save v1 output
00001E2C	07FB			1220+	BR	R11	return
00001E30				1221+RE23	DC	0F	xl16 expected result
00001E30				1222+	DROP	R5	
00001E30	0102F1F2 0304F3F4			1223	DC	XL16' 0102F1F20304F3F4 0506F5F60708F7F8'	result t
00001E38	0506F5F6 0708F7F8						
00001E40	01020304 05060708			1224	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2
00001E48	FFFFFFFF FFFFFFFF						
00001E50	F1F2F3F4 F5F6F7F8			1225	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v3
00001E58	090A0B0C 0D0E0F00						
				1226			
				1227	VRR_C	VMRH, 1	
00001E60				1228+	DS	0FD	
00001E60		00001E60		1229+	USING	*, R5	base for test data and test routine
00001E60	00001EA0			1230+T24	DC	A(X24)	address of test routine
00001E64	0018			1231+	DC	H' 24'	test number
00001E66	00			1232+	DC	X' 00'	
00001E67	01			1233+	DC	HL1' 1'	m4
00001E68	E5D4D9C8 40404040			1234+	DC	CL8' VMRH'	instruction name
00001E70	00001ED8			1235+	DC	A(RE24+16)	address of v2 source
00001E74	00001EE8			1236+	DC	A(RE24+32)	address of v3 source
00001E78	00000010			1237+	DC	A(16)	result length
00001E7C	00001EC8			1238+REA24	DC	A(RE24)	result address
00001E80	00000000 00000000			1239+	DS	FD	gap
00001E88	00000000 00000000			1240+V1024	DS	XL16	V1 output
00001E90	00000000 00000000						
00001E98	00000000 00000000			1241+	DS	FD	gap
				1242+*			
00001EA0				1243+X24	DS	0F	
00001EA0	E310 5010 0014		00000010	1244+	LGF	R1, V2ADDR	load v2 source
00001EA6	E761 0000 0806		00000000	1245+	VL	v22, 0(R1)	use v22 to test decoder
00001EAC	E310 5014 0014		00000014	1246+	LGF	R1, V3ADDR	load v3 source
00001EB2	E771 0000 0806		00000000	1247+	VL	v23, 0(R1)	use v23 to test decoder
00001EB8	E766 7000 1E61			1248+	VMRH	V22, V22, V23, 1	test instruction (dest is a source)
00001EBE	E760 5028 080E		00001E88	1249+	VST	V22, V1024	save v1 output
00001EC4	07FB			1250+	BR	R11	return
00001EC8				1251+RE24	DC	0F	xl16 expected result
00001EC8				1252+	DROP	R5	
00001EC8	F1F20102 F3F40304			1253	DC	XL16' F1F20102F3F40304 F5F60506F7F80708'	result t
00001ED0	F5F60506 F7F80708						
00001ED8	F1F2F3F4 F5F6F7F8			1254	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v2
00001EE0	090A0B0C 0D0E0F00						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001EE8	01020304 05060708			1255	DC	XL16' 0102030405060708 FFFFFFFF' v3	
00001EF0	FFFFFFFF FFFFFFFF						
				1256			
				1257 *Word			
				1258	VRR_C VMRH, 2		
00001EF8				1259+	DS OFD		
00001EF8		00001EF8		1260+	USING *, R5	base for test data and test routine	
00001EF8	00001F38			1261+T25	DC A(X25)	address of test routine	
00001EFC	0019			1262+	DC H' 25'	test number	
00001EFE	00			1263+	DC X' 00'		
00001EFF	02			1264+	DC HL1' 2'	m4	
00001F00	E5D4D9C8 40404040			1265+	DC CL8' VMRH'	instruction name	
00001F08	00001F70			1266+	DC A(RE25+16)	address of v2 source	
00001F0C	00001F80			1267+	DC A(RE25+32)	address of v3 source	
00001F10	00000010			1268+	DC A(16)	result length	
00001F14	00001F60			1269+REA25	DC A(RE25)	result address	
00001F18	00000000 00000000			1270+	DS FD	gap	
00001F20	00000000 00000000			1271+V1025	DS XL16	V1 output	
00001F28	00000000 00000000						
00001F30	00000000 00000000			1272+	DS FD	gap	
				1273+*			
00001F38				1274+X25	DS OF		
00001F38	E310 5010 0014		00000010	1275+	LGF R1, V2ADDR	load v2 source	
00001F3E	E761 0000 0806		00000000	1276+	VL v22, 0(R1)	use v22 to test decoder	
00001F44	E310 5014 0014		00000014	1277+	LGF R1, V3ADDR	load v3 source	
00001F4A	E771 0000 0806		00000000	1278+	VL v23, 0(R1)	use v23 to test decoder	
00001F50	E766 7000 2E61			1279+	VMRH V22, V22, V23, 2	test instruction (dest is a source)	
00001F56	E760 5028 080E		00001F20	1280+	VST V22, V1025	save v1 output	
00001F5C	07FB			1281+	BR R11	return	
00001F60				1282+RE25	DC OF	xl16 expected result	
00001F60				1283+	DROP R5		
00001F60	090A0B0C 01020304			1284	DC XL16' 090A0B0C01020304 0D0E0F0005060708'	result t	
00001F68	0D0E0F00 05060708						
00001F70	090A0B0C 0D0E0F00			1285	DC XL16' 090A0B0C0D0E0F00 FFFFFFFF' v2		
00001F78	FFFFFFFF FFFFFFFF						
00001F80	01020304 05060708			1286	DC XL16' 0102030405060708 090A0B0C0D0E0F00'	v3	
00001F88	090A0B0C 0D0E0F00						
				1287			
				1288	VRR_C VMRH, 2		
00001F90				1289+	DS OFD		
00001F90		00001F90		1290+	USING *, R5	base for test data and test routine	
00001F90	00001FD0			1291+T26	DC A(X26)	address of test routine	
00001F94	001A			1292+	DC H' 26'	test number	
00001F96	00			1293+	DC X' 00'		
00001F97	02			1294+	DC HL1' 2'	m4	
00001F98	E5D4D9C8 40404040			1295+	DC CL8' VMRH'	instruction name	
00001FA0	00002008			1296+	DC A(RE26+16)	address of v2 source	
00001FA4	00002018			1297+	DC A(RE26+32)	address of v3 source	
00001FA8	00000010			1298+	DC A(16)	result length	
00001FAC	00001FF8			1299+REA26	DC A(RE26)	result address	
00001FB0	00000000 00000000			1300+	DS FD	gap	
00001FB8	00000000 00000000			1301+V1026	DS XL16	V1 output	
00001FC0	00000000 00000000						
00001FC8	00000000 00000000			1302+	DS FD	gap	
				1303+*			
00001FD0				1304+X26	DS OF		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001FD0	E310 5010 0014		00000010	1305+	LGF	R1, V2ADDR	load v2 source	
00001FD6	E761 0000 0806		00000000	1306+	VL	v22, 0(R1)	use v22 to test decoder	
00001FDC	E310 5014 0014		00000014	1307+	LGF	R1, V3ADDR	load v3 source	
00001FE2	E771 0000 0806		00000000	1308+	VL	v23, 0(R1)	use v23 to test decoder	
00001FE8	E766 7000 2E61			1309+	VMRH	V22, V22, V23, 2	test instruction (dest is a source)	
00001FEE	E760 5028 080E		00001FB8	1310+	VST	V22, V1026	save v1 output	
00001FF4	07FB			1311+	BR	R11	return	
00001FF8				1312+RE26	DC	0F	xl16 expected result	
00001FF8				1313+	DROP	R5		
00001FF8	01020304 090A0B0C			1314	DC	XL16' 01020304090A0B0C 050607080D0E0F00'	result t	
00002000	05060708 0D0E0F00							
00002008	01020304 05060708			1315	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2	
00002010	FFFFFFFF FFFFFFFF							
00002018	090A0B0C 0D0E0F00			1316	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3	
00002020	01020304 05060708							
				1317				
				1318	VRR_C	VMRH, 2		
00002028				1319+	DS	0FD		
00002028		00002028		1320+	USING	*, R5	base for test data and test routine	
00002028	00002068			1321+T27	DC	A(X27)	address of test routine	
0000202C	001B			1322+	DC	H' 27'	test number	
0000202E	00			1323+	DC	X' 00'		
0000202F	02			1324+	DC	HL1' 2'	m4	
00002030	E5D4D9C8 40404040			1325+	DC	CL8' VMRH'	instruction name	
00002038	000020A0			1326+	DC	A(RE27+16)	address of v2 source	
0000203C	000020B0			1327+	DC	A(RE27+32)	address of v3 source	
00002040	00000010			1328+	DC	A(16)	result length	
00002044	00002090			1329+REA27	DC	A(RE27)	result address	
00002048	00000000 00000000			1330+	DS	FD	gap	
00002050	00000000 00000000			1331+V1027	DS	XL16	V1 output	
00002058	00000000 00000000							
00002060	00000000 00000000			1332+	DS	FD	gap	
				1333+*				
00002068				1334+X27	DS	0F		
00002068	E310 5010 0014		00000010	1335+	LGF	R1, V2ADDR	load v2 source	
0000206E	E761 0000 0806		00000000	1336+	VL	v22, 0(R1)	use v22 to test decoder	
00002074	E310 5014 0014		00000014	1337+	LGF	R1, V3ADDR	load v3 source	
0000207A	E771 0000 0806		00000000	1338+	VL	v23, 0(R1)	use v23 to test decoder	
00002080	E766 7000 2E61			1339+	VMRH	V22, V22, V23, 2	test instruction (dest is a source)	
00002086	E760 5028 080E		00002050	1340+	VST	V22, V1027	save v1 output	
0000208C	07FB			1341+	BR	R11	return	
00002090				1342+RE27	DC	0F	xl16 expected result	
00002090				1343+	DROP	R5		
00002090	01020304 F1F2F3F4			1344	DC	XL16' 01020304F1F2F3F4 05060708F5F6F7F8'	result t	
00002098	05060708 F5F6F7F8							
000020A0	01020304 05060708			1345	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2	
000020A8	FFFFFFFF FFFFFFFF							
000020B0	F1F2F3F4 F5F6F7F8			1346	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v3	
000020B8	090A0B0C 0D0E0F00							
				1347				
				1348	VRR_C	VMRH, 2		
000020C0				1349+	DS	0FD		
000020C0		000020C0		1350+	USING	*, R5	base for test data and test routine	
000020C0	00002100			1351+T28	DC	A(X28)	address of test routine	
000020C4	001C			1352+	DC	H' 28'	test number	
000020C6	00			1353+	DC	X' 00'		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000020C7	02			1354+	DC	HL1' 2'	m4
000020C8	E5D4D9C8 40404040			1355+	DC	CL8' VMRH'	instruction name
000020D0	00002138			1356+	DC	A(RE28+16)	address of v2 source
000020D4	00002148			1357+	DC	A(RE28+32)	address of v3 source
000020D8	00000010			1358+	DC	A(16)	result length
000020DC	00002128			1359+REA28	DC	A(RE28)	result address
000020E0	00000000 00000000			1360+	DS	FD	gap
000020E8	00000000 00000000			1361+V1028	DS	XL16	V1 output
000020F0	00000000 00000000						
000020F8	00000000 00000000			1362+	DS	FD	gap
				1363+*			
00002100				1364+X28	DS	0F	
00002100	E310 5010 0014		00000010	1365+	LGF	R1, V2ADDR	load v2 source
00002106	E761 0000 0806		00000000	1366+	VL	v22, 0(R1)	use v22 to test decoder
0000210C	E310 5014 0014		00000014	1367+	LGF	R1, V3ADDR	load v3 source
00002112	E771 0000 0806		00000000	1368+	VL	v23, 0(R1)	use v23 to test decoder
00002118	E766 7000 2E61			1369+	VMRH	V22, V22, V23, 2	test instruction (dest is a source)
0000211E	E760 5028 080E		000020E8	1370+	VST	V22, V1028	save v1 output
00002124	07FB			1371+	BR	R11	return
00002128				1372+RE28	DC	0F	xl16 expected result
00002128				1373+	DROP	R5	
00002128	F1F2F3F4 01020304			1374	DC	XL16' F1F2F3F401020304 F5F6F7F805060708'	result t
00002130	F5F6F7F8 05060708						
00002138	F1F2F3F4 F5F6F7F8			1375	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v2
00002140	090A0B0C 0D0E0F00						
00002148	01020304 05060708			1376	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v3
00002150	FFFFFFFF FFFFFFFF						
				1377			
				1378 *Doubleword			
00002158				1379	VRR_C	VMRH, 3	
00002158		00002158		1380+	DS	0FD	
00002158	00002198			1381+	USING	*, R5	base for test data and test routine
0000215C	001D			1382+T29	DC	A(X29)	address of test routine
0000215E	00			1383+	DC	H' 29'	test number
0000215F	03			1384+	DC	X' 00'	
00002160	E5D4D9C8 40404040			1385+	DC	HL1' 3'	m4
00002168	000021D0			1386+	DC	CL8' VMRH'	instruction name
0000216C	000021E0			1387+	DC	A(RE29+16)	address of v2 source
00002170	00000010			1388+	DC	A(RE29+32)	address of v3 source
00002174	000021C0			1389+	DC	A(16)	result length
00002178	00000000 00000000			1390+REA29	DC	A(RE29)	result address
00002180	00000000 00000000			1391+	DS	FD	gap
00002188	00000000 00000000			1392+V1029	DS	XL16	V1 output
00002190	00000000 00000000			1393+	DS	FD	gap
				1394+*			
00002198				1395+X29	DS	0F	
00002198	E310 5010 0014		00000010	1396+	LGF	R1, V2ADDR	load v2 source
0000219E	E761 0000 0806		00000000	1397+	VL	v22, 0(R1)	use v22 to test decoder
000021A4	E310 5014 0014		00000014	1398+	LGF	R1, V3ADDR	load v3 source
000021AA	E771 0000 0806		00000000	1399+	VL	v23, 0(R1)	use v23 to test decoder
000021B0	E766 7000 3E61			1400+	VMRH	V22, V22, V23, 3	test instruction (dest is a source)
000021B6	E760 5028 080E		00002180	1401+	VST	V22, V1029	save v1 output
000021BC	07FB			1402+	BR	R11	return
000021C0				1403+RE29	DC	0F	xl16 expected result
000021C0				1404+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000021C0	090A0B0C 0D0E0F00			1405	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	result
000021C8	01020304 05060708						
000021D0	090A0B0C 0D0E0F00			1406	DC	XL16' 090A0B0C0D0E0F00 FFFFFFFFFFFFFFFF'	v2
000021D8	FFFFFFFF FFFFFFFF						
000021E0	01020304 05060708			1407	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
000021E8	090A0B0C 0D0E0F00						
				1408			
				1409	VRR_C	VMRH, 3	
000021F0				1410+	DS	OFD	
000021F0		000021F0		1411+	USING	*, R5	base for test data and test routine
000021F0	00002230			1412+T30	DC	A(X30)	address of test routine
000021F4	001E			1413+	DC	H' 30'	test number
000021F6	00			1414+	DC	X' 00'	
000021F7	03			1415+	DC	HL1' 3'	m4
000021F8	E5D4D9C8 40404040			1416+	DC	CL8' VMRH'	instruction name
00002200	00002268			1417+	DC	A(RE30+16)	address of v2 source
00002204	00002278			1418+	DC	A(RE30+32)	address of v3 source
00002208	00000010			1419+	DC	A(16)	result length
0000220C	00002258			1420+REA30	DC	A(RE30)	result address
00002210	00000000 00000000			1421+	DS	FD	gap
00002218	00000000 00000000			1422+V1030	DS	XL16	V1 output
00002220	00000000 00000000						
00002228	00000000 00000000			1423+	DS	FD	gap
				1424+*			
00002230				1425+X30	DS	OF	
00002230	E310 5010 0014		00000010	1426+	LGF	R1, V2ADDR	load v2 source
00002236	E761 0000 0806		00000000	1427+	VL	v22, 0(R1)	use v22 to test decoder
0000223C	E310 5014 0014		00000014	1428+	LGF	R1, V3ADDR	load v3 source
00002242	E771 0000 0806		00000000	1429+	VL	v23, 0(R1)	use v23 to test decoder
00002248	E766 7000 3E61			1430+	VMRH	V22, V22, V23, 3	test instruction (dest is a source)
0000224E	E760 A018 080E		00002218	1431+	VST	V22, V1030	save v1 output
00002254	07FB			1432+	BR	R11	return
00002258				1433+RE30	DC	OF	xl16 expected result
00002258				1434+	DROP	R5	
00002258	01020304 05060708			1435	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	result
00002260	090A0B0C 0D0E0F00						
00002268	01020304 05060708			1436	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFF'	v2
00002270	FFFFFFFF FFFFFFFF						
00002278	090A0B0C 0D0E0F00			1437	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3
00002280	01020304 05060708						
				1438			
				1439	VRR_C	VMRH, 3	
00002288				1440+	DS	OFD	
00002288		00002288		1441+	USING	*, R5	base for test data and test routine
00002288	000022C8			1442+T31	DC	A(X31)	address of test routine
0000228C	001F			1443+	DC	H' 31'	test number
0000228E	00			1444+	DC	X' 00'	
0000228F	03			1445+	DC	HL1' 3'	m4
00002290	E5D4D9C8 40404040			1446+	DC	CL8' VMRH'	instruction name
00002298	00002300			1447+	DC	A(RE31+16)	address of v2 source
0000229C	00002310			1448+	DC	A(RE31+32)	address of v3 source
000022A0	00000010			1449+	DC	A(16)	result length
000022A4	000022F0			1450+REA31	DC	A(RE31)	result address
000022A8	00000000 00000000			1451+	DS	FD	gap
000022B0	00000000 00000000			1452+V1031	DS	XL16	V1 output
000022B8	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000022C0	00000000 00000000			1453+	DS	FD	gap	
				1454+*				
000022C8				1455+X31	DS	0F		
000022C8	E310 5010 0014		00000010	1456+	LGF	R1, V2ADDR	load v2 source	
000022CE	E761 0000 0806		00000000	1457+	VL	v22, 0(R1)	use v22 to test decoder	
000022D4	E310 5014 0014		00000014	1458+	LGF	R1, V3ADDR	load v3 source	
000022DA	E771 0000 0806		00000000	1459+	VL	v23, 0(R1)	use v23 to test decoder	
000022E0	E766 7000 3E61			1460+	VMRH	V22, V22, V23, 3	test instruction (dest is a source)	
000022E6	E760 5028 080E		000022B0	1461+	VST	V22, V1031	save v1 output	
000022EC	07FB			1462+	BR	R11	return	
000022F0				1463+RE31	DC	0F	xl16 expected result	
000022F0				1464+	DROP	R5		
000022F0	01020304 05060708			1465	DC	XL16' 0102030405060708 F1F2F3F4F5F6F7F8'	result t	
000022F8	F1F2F3F4 F5F6F7F8							
00002300	01020304 05060708			1466	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2	
00002308	FFFFFFFF FFFFFFFFFF							
00002310	F1F2F3F4 F5F6F7F8			1467	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v3	
00002318	090A0B0C 0D0E0F00							
				1468				
				1469	VRR_C	VMRH, 3		
00002320				1470+	DS	0FD		
00002320		00002320		1471+	USING	*, R5	base for test data and test routine	
00002320	00002360			1472+T32	DC	A(X32)	address of test routine	
00002324	0020			1473+	DC	H' 32'	test number	
00002326	00			1474+	DC	X' 00'		
00002327	03			1475+	DC	HL1' 3'	m4	
00002328	E5D4D9C8 40404040			1476+	DC	CL8' VMRH'	instruction name	
00002330	00002398			1477+	DC	A(RE32+16)	address of v2 source	
00002334	000023A8			1478+	DC	A(RE32+32)	address of v3 source	
00002338	00000010			1479+	DC	A(16)	result length	
0000233C	00002388			1480+REA32	DC	A(RE32)	result address	
00002340	00000000 00000000			1481+	DS	FD	gap	
00002348	00000000 00000000			1482+V1032	DS	XL16	V1 output	
00002350	00000000 00000000							
00002358	00000000 00000000			1483+	DS	FD	gap	
				1484+*				
00002360				1485+X32	DS	0F		
00002360	E310 5010 0014		00000010	1486+	LGF	R1, V2ADDR	load v2 source	
00002366	E761 0000 0806		00000000	1487+	VL	v22, 0(R1)	use v22 to test decoder	
0000236C	E310 5014 0014		00000014	1488+	LGF	R1, V3ADDR	load v3 source	
00002372	E771 0000 0806		00000000	1489+	VL	v23, 0(R1)	use v23 to test decoder	
00002378	E766 7000 3E61			1490+	VMRH	V22, V22, V23, 3	test instruction (dest is a source)	
0000237E	E760 5028 080E		00002348	1491+	VST	V22, V1032	save v1 output	
00002384	07FB			1492+	BR	R11	return	
00002388				1493+RE32	DC	0F	xl16 expected result	
00002388				1494+	DROP	R5		
00002388	F1F2F3F4 F5F6F7F8			1495	DC	XL16' F1F2F3F4F5F6F7F8 0102030405060708'	result t	
00002390	01020304 05060708							
00002398	F1F2F3F4 F5F6F7F8			1496	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v2	
000023A0	090A0B0C 0D0E0F00							
000023A8	01020304 05060708			1497	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v3	
000023B0	FFFFFFFF FFFFFFFFFF							
				1498				
				1499				
				1500 *				
				1501 *	VPK	- Vector Pack		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1502 *-----	
				1503 *Halfword	
000023B8				1504 VRR_C VPK, 1	
000023B8		000023B8		1505+ DS OFD	
000023B8	000023F8			1506+ USING *, R5	base for test data and test routine
000023BC	0021			1507+T33 DC A(X33)	address of test routine
000023BE	00			1508+ DC H' 33'	test number
000023BF	01			1509+ DC X' 00'	
000023C0	E5D7D240 40404040			1510+ DC HL1' 1'	m4
000023C8	00002430			1511+ DC CL8' VPK'	instruction name
000023CC	00002440			1512+ DC A(RE33+16)	address of v2 source
000023D0	00000010			1513+ DC A(RE33+32)	address of v3 source
000023D4	00002420			1514+ DC A(16)	result length
000023D8	00000000 00000000			1515+REA33 DC A(RE33)	result address
000023E0	00000000 00000000			1516+ DS FD	gap
000023E8	00000000 00000000			1517+V1033 DS XL16	V1 output
000023F0	00000000 00000000			1518+ DS FD	gap
				1519+*	
000023F8				1520+X33 DS OF	
000023F8	E310 5010 0014	00000010		1521+ LGF R1, V2ADDR	load v2 source
000023FE	E761 0000 0806	00000000		1522+ VL v22, 0(R1)	use v22 to test decoder
00002404	E310 5014 0014	00000014		1523+ LGF R1, V3ADDR	load v3 source
0000240A	E771 0000 0806	00000000		1524+ VL v23, 0(R1)	use v23 to test decoder
00002410	E766 7000 1E94			1525+ VPK V22, V22, V23, 1	test instruction (dest is a source)
00002416	E760 5028 080E	000023E0		1526+ VST V22, V1033	save v1 output
0000241C	07FB			1527+ BR R11	return
00002420				1528+RE33 DC OF	xl16 expected result
00002420				1529+ DROP R5	
00002420	0A0C0E00 FFFFFFFF			1530 DC XL16' 0A0C0E00FFFFFFFF 020406080A0C0E00'	result
00002428	02040608 0A0C0E00				
00002430	090A0B0C 0D0E0F00			1531 DC XL16' 090A0B0C0D0E0F00 FFFFFFFFFFFFFFFFFF'	v2
00002438	FFFFFFFF FFFFFFFF				
00002440	01020304 05060708			1532 DC XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
00002448	090A0B0C 0D0E0F00				
				1533	
00002450				1534 VRR_C VPK, 1	
00002450		00002450		1535+ DS OFD	
00002450	00002490			1536+ USING *, R5	base for test data and test routine
00002454	0022			1537+T34 DC A(X34)	address of test routine
00002456	00			1538+ DC H' 34'	test number
00002457	01			1539+ DC X' 00'	
00002458	E5D7D240 40404040			1540+ DC HL1' 1'	m4
00002460	000024C8			1541+ DC CL8' VPK'	instruction name
00002464	000024D8			1542+ DC A(RE34+16)	address of v2 source
00002468	00000010			1543+ DC A(RE34+32)	address of v3 source
0000246C	000024B8			1544+ DC A(16)	result length
00002470	00000000 00000000			1545+REA34 DC A(RE34)	result address
00002478	00000000 00000000			1546+ DS FD	gap
00002480	00000000 00000000			1547+V1034 DS XL16	V1 output
00002488	00000000 00000000			1548+ DS FD	gap
				1549+*	
00002490				1550+X34 DS OF	
00002490	E310 5010 0014	00000010		1551+ LGF R1, V2ADDR	load v2 source
00002496	E761 0000 0806	00000000		1552+ VL v22, 0(R1)	use v22 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000249C	E310 5014 0014		00000014	1553+	LGF	R1, V3ADDR	load v3 source
000024A2	E771 0000 0806		00000000	1554+	VL	v23, 0(R1)	use v23 to test decoder
000024A8	E766 7000 1E94			1555+	VPK	V22, V22, V23, 1	test instruction (dest is a source)
000024AE	E760 5028 080E		00002478	1556+	VST	V22, V1034	save v1 output
000024B4	07FB			1557+	BR	R11	return
000024B8				1558+RE34	DC	0F	xl16 expected result
000024B8				1559+	DROP	R5	
000024B8	02040608 FFFFFFFF			1560	DC	XL16' 02040608FFFFFFFF 0A0C0E0002040608'	result t
000024C0	0A0C0E00 02040608						
000024C8	01020304 05060708			1561	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2
000024D0	FFFFFFFF FFFFFFFF						
000024D8	090A0B0C 0D0E0F00			1562	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3
000024E0	01020304 05060708						
				1563			
000024E8				1564	VRR_C	VPK, 1	
000024E8		000024E8		1565+	DS	0FD	
000024E8	00002528			1566+	USING	*, R5	base for test data and test routine
000024EC	0023			1567+T35	DC	A(X35)	address of test routine
000024EE	00			1568+	DC	H' 35'	test number
000024EF	01			1569+	DC	X' 00'	
000024F0	E5D7D240 40404040			1570+	DC	HL1' 1'	m4
000024F8	00002560			1571+	DC	CL8' VPK'	instruction name
000024FC	00002570			1572+	DC	A(RE35+16)	address of v2 source
00002500	00000010			1573+	DC	A(RE35+32)	address of v3 source
00002504	00002550			1574+	DC	A(16)	result length
00002508	00000000 00000000			1575+REA35	DC	A(RE35)	result address
00002510	00000000 00000000			1576+	DS	FD	gap
00002518	00000000 00000000			1577+V1035	DS	XL16	V1 output
00002520	00000000 00000000						
				1578+	DS	FD	gap
				1579+*			
00002528				1580+X35	DS	0F	
00002528	E310 5010 0014		00000010	1581+	LGF	R1, V2ADDR	load v2 source
0000252E	E761 0000 0806		00000000	1582+	VL	v22, 0(R1)	use v22 to test decoder
00002534	E310 5014 0014		00000014	1583+	LGF	R1, V3ADDR	load v3 source
0000253A	E771 0000 0806		00000000	1584+	VL	v23, 0(R1)	use v23 to test decoder
00002540	E766 7000 1E94			1585+	VPK	V22, V22, V23, 1	test instruction (dest is a source)
00002546	E760 5028 080E		00002510	1586+	VST	V22, V1035	save v1 output
0000254C	07FB			1587+	BR	R11	return
00002550				1588+RE35	DC	0F	xl16 expected result
00002550				1589+	DROP	R5	
00002550	02040608 FFFFFFFF			1590	DC	XL16' 02040608FFFFFFFF F2F4F6F80A0C0E00'	result t
00002558	F2F4F6F8 0A0C0E00						
00002560	01020304 05060708			1591	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2
00002568	FFFFFFFF FFFFFFFF						
00002570	F1F2F3F4 F5F6F7F8			1592	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v3
00002578	090A0B0C 0D0E0F00						
				1593			
00002580				1594	VRR_C	VPK, 1	
00002580		00002580		1595+	DS	0FD	
00002580	000025C0			1596+	USING	*, R5	base for test data and test routine
00002584	0024			1597+T36	DC	A(X36)	address of test routine
00002586	00			1598+	DC	H' 36'	test number
00002587	01			1599+	DC	X' 00'	
00002588	E5D7D240 40404040			1600+	DC	HL1' 1'	m4
				1601+	DC	CL8' VPK'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002590	000025F8			1602+	DC	A(RE36+16)	address of v2 source
00002594	00002608			1603+	DC	A(RE36+32)	address of v3 source
00002598	00000010			1604+	DC	A(16)	result length
0000259C	000025E8			1605+REA36	DC	A(RE36)	result address
000025A0	00000000 00000000			1606+	DS	FD	gap
000025A8	00000000 00000000			1607+V1036	DS	XL16	V1 output
000025B0	00000000 00000000						
000025B8	00000000 00000000			1608+	DS	FD	gap
				1609+*			
000025C0				1610+X36	DS	0F	
000025C0	E310 5010 0014		00000010	1611+	LGF	R1, V2ADDR	load v2 source
000025C6	E761 0000 0806		00000000	1612+	VL	v22, 0(R1)	use v22 to test decoder
000025CC	E310 5014 0014		00000014	1613+	LGF	R1, V3ADDR	load v3 source
000025D2	E771 0000 0806		00000000	1614+	VL	v23, 0(R1)	use v23 to test decoder
000025D8	E766 7000 1E94			1615+	VPK	V22, V22, V23, 1	test instruction (dest is a source)
000025DE	E760 5028 080E		000025A8	1616+	VST	V22, V1036	save v1 output
000025E4	07FB			1617+	BR	R11	return
000025E8				1618+RE36	DC	0F	xl16 expected result
000025E8				1619+	DROP	R5	
000025E8	F2F4F6F8 0A0C0E00			1620	DC	XL16' F2F4F6F80A0C0E00 02040608FFFFFFFF'	result t
000025F0	02040608 FFFFFFFF						
000025F8	F1F2F3F4 F5F6F7F8			1621	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v2
00002600	090A0B0C 0D0E0F00						
00002608	01020304 05060708			1622	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v3
00002610	FFFFFFFF FFFFFFFF						
				1623			
				1624 *Word			
				1625	VRR_C	VPK, 2	
00002618				1626+	DS	0FD	
00002618		00002618		1627+	USING	*, R5	base for test data and test routine
00002618	00002658			1628+T37	DC	A(X37)	address of test routine
0000261C	0025			1629+	DC	H' 37'	test number
0000261E	00			1630+	DC	X' 00'	
0000261F	02			1631+	DC	HL1' 2'	m4
00002620	E5D7D240 40404040			1632+	DC	CL8' VPK'	instruction name
00002628	00002690			1633+	DC	A(RE37+16)	address of v2 source
0000262C	000026A0			1634+	DC	A(RE37+32)	address of v3 source
00002630	00000010			1635+	DC	A(16)	result length
00002634	00002680			1636+REA37	DC	A(RE37)	result address
00002638	00000000 00000000			1637+	DS	FD	gap
00002640	00000000 00000000			1638+V1037	DS	XL16	V1 output
00002648	00000000 00000000						
00002650	00000000 00000000			1639+	DS	FD	gap
				1640+*			
00002658				1641+X37	DS	0F	
00002658	E310 5010 0014		00000010	1642+	LGF	R1, V2ADDR	load v2 source
0000265E	E761 0000 0806		00000000	1643+	VL	v22, 0(R1)	use v22 to test decoder
00002664	E310 5014 0014		00000014	1644+	LGF	R1, V3ADDR	load v3 source
0000266A	E771 0000 0806		00000000	1645+	VL	v23, 0(R1)	use v23 to test decoder
00002670	E766 7000 2E94			1646+	VPK	V22, V22, V23, 2	test instruction (dest is a source)
00002676	E760 5028 080E		00002640	1647+	VST	V22, V1037	save v1 output
0000267C	07FB			1648+	BR	R11	return
00002680				1649+RE37	DC	0F	xl16 expected result
00002680				1650+	DROP	R5	
00002680	0B0C0F00 FFFFFFFF			1651	DC	XL16' 0B0C0F00FFFFFFFF 030407080B0C0F00'	result t
00002688	03040708 0B0C0F00						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002690	090A0B0C 0D0E0F00			1652	DC	XL16' 090A0B0C0D0E0F00 FFFFFFFFFFFFFFFF'	v2
00002698	FFFFFFFF FFFFFFFF						
000026A0	01020304 05060708			1653	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
000026A8	090A0B0C 0D0E0F00						
				1654			
000026B0				1655	VRR_C	VPK, 2	
000026B0		000026B0		1656+	DS	OFD	
000026B0	000026F0			1657+	USING	*, R5	base for test data and test routine
000026B4	0026			1658+T38	DC	A(X38)	address of test routine
000026B6	00			1659+	DC	H' 38'	test number
000026B7	02			1660+	DC	X' 00'	
000026B8	E5D7D240 40404040			1661+	DC	HL1' 2'	m4
000026C0	00002728			1662+	DC	CL8' VPK'	instruction name
000026C4	00002738			1663+	DC	A(RE38+16)	address of v2 source
000026C8	00000010			1664+	DC	A(RE38+32)	address of v3 source
000026CC	00002718			1665+	DC	A(16)	result length
000026D0	00000000 00000000			1666+REA38	DC	A(RE38)	result address
000026D8	00000000 00000000			1667+	DS	FD	gap
000026E0	00000000 00000000			1668+V1038	DS	XL16	V1 output
000026E8	00000000 00000000			1669+	DS	FD	gap
				1670+*			
000026F0				1671+X38	DS	OF	
000026F0	E310 5010 0014		00000010	1672+	LGF	R1, V2ADDR	load v2 source
000026F6	E761 0000 0806		00000000	1673+	VL	v22, 0(R1)	use v22 to test decoder
000026FC	E310 5014 0014		00000014	1674+	LGF	R1, V3ADDR	load v3 source
00002702	E771 0000 0806		00000000	1675+	VL	v23, 0(R1)	use v23 to test decoder
00002708	E766 7000 2E94			1676+	VPK	V22, V22, V23, 2	test instruction (dest is a source)
0000270E	E760 5028 080E		000026D8	1677+	VST	V22, V1038	save v1 output
00002714	07FB			1678+	BR	R11	return
00002718				1679+RE38	DC	OF	xl16 expected result
00002718				1680+	DROP	R5	
00002718	03040708 FFFFFFFF			1681	DC	XL16' 03040708FFFFFFFF 0B0C0F0003040708'	result t
00002720	0B0C0F00 03040708						
00002728	01020304 05060708			1682	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFF'	v2
00002730	FFFFFFFF FFFFFFFF						
00002738	090A0B0C 0D0E0F00			1683	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3
00002740	01020304 05060708						
				1684			
00002748				1685	VRR_C	VPK, 2	
00002748		00002748		1686+	DS	OFD	
00002748	00002788			1687+	USING	*, R5	base for test data and test routine
0000274C	0027			1688+T39	DC	A(X39)	address of test routine
0000274E	00			1689+	DC	H' 39'	test number
0000274F	02			1690+	DC	X' 00'	
00002750	E5D7D240 40404040			1691+	DC	HL1' 2'	m4
00002758	000027C0			1692+	DC	CL8' VPK'	instruction name
0000275C	000027D0			1693+	DC	A(RE39+16)	address of v2 source
00002760	00000010			1694+	DC	A(RE39+32)	address of v3 source
00002764	000027B0			1695+	DC	A(16)	result length
00002768	00000000 00000000			1696+REA39	DC	A(RE39)	result address
00002770	00000000 00000000			1697+	DS	FD	gap
00002778	00000000 00000000			1698+V1039	DS	XL16	V1 output
00002780	00000000 00000000			1699+	DS	FD	gap
				1700+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002788				1701+X39	DS	0F	
00002788	E310 5010 0014		00000010	1702+	LGF	R1, V2ADDR	load v2 source
0000278E	E761 0000 0806		00000000	1703+	VL	v22, 0(R1)	use v22 to test decoder
00002794	E310 5014 0014		00000014	1704+	LGF	R1, V3ADDR	load v3 source
0000279A	E771 0000 0806		00000000	1705+	VL	v23, 0(R1)	use v23 to test decoder
000027A0	E766 7000 2E94			1706+	VPK	V22, V22, V23, 2	test instruction (dest is a source)
000027A6	E760 5028 080E		00002770	1707+	VST	V22, V1039	save v1 output
000027AC	07FB			1708+	BR	R11	return
000027B0				1709+RE39	DC	0F	xl16 expected result
000027B0				1710+	DROP	R5	
000027B0	03040708 FFFFFFFF			1711	DC	XL16' 03040708FFFFFFFF F3F4F7F80B0C0F00'	result t
000027B8	F3F4F7F8 0B0C0F00						
000027C0	01020304 05060708			1712	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2
000027C8	FFFFFFFF FFFFFFFF						
000027D0	F1F2F3F4 F5F6F7F8			1713	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v3
000027D8	090A0B0C 0D0E0F00						
				1714			
000027E0				1715	VRR_C	VPK, 2	
000027E0		000027E0		1716+	DS	0FD	
000027E0	00002820			1717+	USING	*, R5	base for test data and test routine
000027E4	0028			1718+T40	DC	A(X40)	address of test routine
000027E6	00			1719+	DC	H' 40'	test number
000027E7	02			1720+	DC	X' 00'	
000027E8	E5D7D240 40404040			1721+	DC	HL1' 2'	m4
000027F0	00002858			1722+	DC	CL8' VPK'	instruction name
000027F4	00002868			1723+	DC	A(RE40+16)	address of v2 source
000027F8	00000010			1724+	DC	A(RE40+32)	address of v3 source
000027FC	00002848			1725+	DC	A(16)	result length
00002800	00000000 00000000			1726+REA40	DC	A(RE40)	result address
00002808	00000000 00000000			1727+	DS	FD	gap
00002810	00000000 00000000			1728+V1040	DS	XL16	V1 output
00002818	00000000 00000000						
				1729+	DS	FD	gap
				1730+*			
00002820				1731+X40	DS	0F	
00002820	E310 5010 0014		00000010	1732+	LGF	R1, V2ADDR	load v2 source
00002826	E761 0000 0806		00000000	1733+	VL	v22, 0(R1)	use v22 to test decoder
0000282C	E310 5014 0014		00000014	1734+	LGF	R1, V3ADDR	load v3 source
00002832	E771 0000 0806		00000000	1735+	VL	v23, 0(R1)	use v23 to test decoder
00002838	E766 7000 2E94			1736+	VPK	V22, V22, V23, 2	test instruction (dest is a source)
0000283E	E760 5028 080E		00002808	1737+	VST	V22, V1040	save v1 output
00002844	07FB			1738+	BR	R11	return
00002848				1739+RE40	DC	0F	xl16 expected result
00002848				1740+	DROP	R5	
00002848	F3F4F7F8 0B0C0F00			1741	DC	XL16' F3F4F7F80B0C0F00 03040708FFFFFFFF'	result t
00002850	03040708 FFFFFFFF						
00002858	F1F2F3F4 F5F6F7F8			1742	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v2
00002860	090A0B0C 0D0E0F00						
00002868	01020304 05060708			1743	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v3
00002870	FFFFFFFF FFFFFFFF						
				1744			
				1745 *Doubleword			
				1746	VRR_C	VPK, 3	
00002878				1747+	DS	0FD	
00002878		00002878		1748+	USING	*, R5	base for test data and test routine
00002878	000028B8			1749+T41	DC	A(X41)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000287C	0029			1750+	DC	H' 41'	test number
0000287E	00			1751+	DC	X' 00'	
0000287F	03			1752+	DC	HL1' 3'	m4
00002880	E5D7D240 40404040			1753+	DC	CL8' VPK'	instruction name
00002888	000028F0			1754+	DC	A(RE41+16)	address of v2 source
0000288C	00002900			1755+	DC	A(RE41+32)	address of v3 source
00002890	00000010			1756+	DC	A(16)	result length
00002894	000028E0			1757+REA41	DC	A(RE41)	result address
00002898	00000000 00000000			1758+	DS	FD	gap
000028A0	00000000 00000000			1759+V1041	DS	XL16	V1 output
000028A8	00000000 00000000						
000028B0	00000000 00000000			1760+	DS	FD	gap
				1761+*			
000028B8				1762+X41	DS	0F	
000028B8	E310 5010 0014		00000010	1763+	LGF	R1, V2ADDR	load v2 source
000028BE	E761 0000 0806		00000000	1764+	VL	v22, 0(R1)	use v22 to test decoder
000028C4	E310 5014 0014		00000014	1765+	LGF	R1, V3ADDR	load v3 source
000028CA	E771 0000 0806		00000000	1766+	VL	v23, 0(R1)	use v23 to test decoder
000028D0	E766 7000 3E94			1767+	VPK	V22, V22, V23, 3	test instruction (dest is a source)
000028D6	E760 5028 080E		000028A0	1768+	VST	V22, V1041	save v1 output
000028DC	07FB			1769+	BR	R11	return
000028E0				1770+RE41	DC	0F	xl16 expected result
000028E0				1771+	DROP	R5	
000028E0	0D0E0F00 FFFFFFFF			1772	DC	XL16' 0D0E0F00FFFFFFFF 050607080D0E0F00'	result t
000028E8	05060708 0D0E0F00						
000028F0	090A0B0C 0D0E0F00			1773	DC	XL16' 090A0B0C0D0E0F00 FFFFFFFFFFFFFFFFFF'	v2
000028F8	FFFFFFFF FFFFFFFF						
00002900	01020304 05060708			1774	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	v3
00002908	090A0B0C 0D0E0F00						
				1775			
00002910				1776	VRR_C	VPK, 3	
00002910		00002910		1777+	DS	0FD	
00002910	00002950			1778+	USING	*, R5	base for test data and test routine
00002914	002A			1779+T42	DC	A(X42)	address of test routine
00002916	00			1780+	DC	H' 42'	test number
00002917	03			1781+	DC	X' 00'	
00002917	03			1782+	DC	HL1' 3'	m4
00002918	E5D7D240 40404040			1783+	DC	CL8' VPK'	instruction name
00002920	00002988			1784+	DC	A(RE42+16)	address of v2 source
00002924	00002998			1785+	DC	A(RE42+32)	address of v3 source
00002928	00000010			1786+	DC	A(16)	result length
0000292C	00002978			1787+REA42	DC	A(RE42)	result address
00002930	00000000 00000000			1788+	DS	FD	gap
00002938	00000000 00000000			1789+V1042	DS	XL16	V1 output
00002940	00000000 00000000						
00002948	00000000 00000000			1790+	DS	FD	gap
				1791+*			
00002950				1792+X42	DS	0F	
00002950	E310 5010 0014		00000010	1793+	LGF	R1, V2ADDR	load v2 source
00002956	E761 0000 0806		00000000	1794+	VL	v22, 0(R1)	use v22 to test decoder
0000295C	E310 5014 0014		00000014	1795+	LGF	R1, V3ADDR	load v3 source
00002962	E771 0000 0806		00000000	1796+	VL	v23, 0(R1)	use v23 to test decoder
00002968	E766 7000 3E94			1797+	VPK	V22, V22, V23, 3	test instruction (dest is a source)
0000296E	E760 5028 080E		00002938	1798+	VST	V22, V1042	save v1 output
00002974	07FB			1799+	BR	R11	return
00002978				1800+RE42	DC	0F	xl16 expected result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002978				1801+	DROP	R5	
00002978	05060708 FFFFFFFF			1802	DC	XL16' 05060708FFFFFFFF 0D0E0F0005060708'	result
00002980	0D0E0F00 05060708						
00002988	01020304 05060708			1803	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2
00002990	FFFFFFFF FFFFFFFF						
00002998	090A0B0C 0D0E0F00			1804	DC	XL16' 090A0B0C0D0E0F00 0102030405060708'	v3
000029A0	01020304 05060708						
				1805			
000029A8				1806	VRR_C	VPK, 3	
000029A8		000029A8		1807+	DS	0FD	
000029A8	000029E8			1808+	USING	*, R5	base for test data and test routine
000029AC	002B			1809+T43	DC	A(X43)	address of test routine
000029AE	00			1810+	DC	H' 43'	test number
000029AF	03			1811+	DC	X' 00'	
000029B0	E5D7D240 40404040			1812+	DC	HL1' 3'	m4
000029B8	00002A20			1813+	DC	CL8' VPK'	instruction name
000029BC	00002A30			1814+	DC	A(RE43+16)	address of v2 source
000029C0	00000010			1815+	DC	A(RE43+32)	address of v3 source
000029C4	00002A10			1816+	DC	A(16)	result length
000029C8	00000000 00000000			1817+REA43	DC	A(RE43)	result address
000029D0	00000000 00000000			1818+	DS	FD	gap
000029D8	00000000 00000000			1819+V1043	DS	XL16	V1 output
000029E0	00000000 00000000						
				1820+	DS	FD	gap
				1821+*			
000029E8				1822+X43	DS	0F	
000029E8	E310 5010 0014		00000010	1823+	LGF	R1, V2ADDR	load v2 source
000029EE	E761 0000 0806		00000000	1824+	VL	v22, 0(R1)	use v22 to test decoder
000029F4	E310 5014 0014		00000014	1825+	LGF	R1, V3ADDR	load v3 source
000029FA	E771 0000 0806		00000000	1826+	VL	v23, 0(R1)	use v23 to test decoder
00002A00	E766 7000 3E94			1827+	VPK	V22, V22, V23, 3	test instruction (dest is a source)
00002A06	E760 5028 080E		000029D0	1828+	VST	V22, V1043	save v1 output
00002A0C	07FB			1829+	BR	R11	return
00002A10				1830+RE43	DC	0F	xl16 expected result
00002A10				1831+	DROP	R5	
00002A10	05060708 FFFFFFFF			1832	DC	XL16' 05060708FFFFFFFF F5F6F7F80D0E0F00'	result
00002A18	F5F6F7F8 0D0E0F00						
00002A20	01020304 05060708			1833	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v2
00002A28	FFFFFFFF FFFFFFFF						
00002A30	F1F2F3F4 F5F6F7F8			1834	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0C0D0E0F00'	v3
00002A38	090A0B0C 0D0E0F00						
				1835			
00002A40				1836	VRR_C	VPK, 3	
00002A40		00002A40		1837+	DS	0FD	
00002A40	00002A80			1838+	USING	*, R5	base for test data and test routine
00002A44	002C			1839+T44	DC	A(X44)	address of test routine
00002A46	00			1840+	DC	H' 44'	test number
00002A47	03			1841+	DC	X' 00'	
00002A48	E5D7D240 40404040			1842+	DC	HL1' 3'	m4
00002A50	00002AB8			1843+	DC	CL8' VPK'	instruction name
00002A54	00002AC8			1844+	DC	A(RE44+16)	address of v2 source
00002A58	00000010			1845+	DC	A(RE44+32)	address of v3 source
00002A5C	00002AA8			1846+	DC	A(16)	result length
00002A60	00000000 00000000			1847+REA44	DC	A(RE44)	result address
00002A68	00000000 00000000			1848+	DS	FD	gap
				1849+V1044	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002A70	00000000 00000000							
00002A78	00000000 00000000			1850+	DS	FD	gap	
				1851+*				
00002A80				1852+X44	DS	0F		
00002A80	E310 5010 0014		00000010	1853+	LGF	R1, V2ADDR	load v2 source	
00002A86	E761 0000 0806		00000000	1854+	VL	v22, 0(R1)	use v22 to test decoder	
00002A8C	E310 5014 0014		00000014	1855+	LGF	R1, V3ADDR	load v3 source	
00002A92	E771 0000 0806		00000000	1856+	VL	v23, 0(R1)	use v23 to test decoder	
00002A98	E766 7000 3E94			1857+	VPK	V22, V22, V23, 3	test instruction (dest is a source)	
00002A9E	E760 5028 080E		00002A68	1858+	VST	V22, V1044	save v1 output	
00002AA4	07FB			1859+	BR	R11	return	
00002AA8				1860+RE44	DC	0F	xl16 expected result	
00002AA8				1861+	DROP	R5		
00002AA8	F5F6F7F8 F5F6F7F8			1862	DC	XL16' F5F6F7F8F5F6F7F8 05060708FFFFFFFF'	result t	
00002AB0	05060708 FFFFFFFF							
00002AB8	F1F2F3F4 F5F6F7F8			1863	DC	XL16' F1F2F3F4F5F6F7F8 090A0B0CF5F6F7F8'	v2	
00002AC0	090A0B0C F5F6F7F8							
00002AC8	01020304 05060708			1864	DC	XL16' 0102030405060708 FFFFFFFFFFFFFFFFFF'	v3	
00002AD0	FFFFFFFF FFFFFFFF							
				1865				
				1866				
00002AD8	00000000			1867	DC	F' 0'	END OF TABLE	
00002ADC	00000000			1868	DC	F' 0'		
				1869 *				
				1870 *			table of pointers to individual load test	
				1871 *				
00002AE0				1872 E7TESTS	DS	0F		
				1873	PTTABLE			
00002AE0				1874+TTABLE	DS	0F		
00002AE0	000010B8			1875+	DC	A(T1)		
00002AE4	00001150			1876+	DC	A(T2)		
00002AE8	000011E8			1877+	DC	A(T3)		
00002AEC	00001280			1878+	DC	A(T4)		
00002AF0	00001318			1879+	DC	A(T5)		
00002AF4	000013B0			1880+	DC	A(T6)		
00002AF8	00001448			1881+	DC	A(T7)		
00002AFC	000014E0			1882+	DC	A(T8)		
00002B00	00001578			1883+	DC	A(T9)		
00002B04	00001610			1884+	DC	A(T10)		
00002B08	000016A8			1885+	DC	A(T11)		
00002B0C	00001740			1886+	DC	A(T12)		
00002B10	000017D8			1887+	DC	A(T13)		
00002B14	00001870			1888+	DC	A(T14)		
00002B18	00001908			1889+	DC	A(T15)		
00002B1C	000019A0			1890+	DC	A(T16)		
00002B20	00001A38			1891+	DC	A(T17)		
00002B24	00001AD0			1892+	DC	A(T18)		
00002B28	00001B68			1893+	DC	A(T19)		
00002B2C	00001C00			1894+	DC	A(T20)		
00002B30	00001C98			1895+	DC	A(T21)		
00002B34	00001D30			1896+	DC	A(T22)		
00002B38	00001DC8			1897+	DC	A(T23)		
00002B3C	00001E60			1898+	DC	A(T24)		
00002B40	00001EF8			1899+	DC	A(T25)		
00002B44	00001F90			1900+	DC	A(T26)		
00002B48	00002028			1901+	DC	A(T27)		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1926	*****	
				1927	* Register equates	
				1928	*****	
		00000000	00000001	1930 R0	EQU	0
		00000001	00000001	1931 R1	EQU	1
		00000002	00000001	1932 R2	EQU	2
		00000003	00000001	1933 R3	EQU	3
		00000004	00000001	1934 R4	EQU	4
		00000005	00000001	1935 R5	EQU	5
		00000006	00000001	1936 R6	EQU	6
		00000007	00000001	1937 R7	EQU	7
		00000008	00000001	1938 R8	EQU	8
		00000009	00000001	1939 R9	EQU	9
		0000000A	00000001	1940 R10	EQU	10
		0000000B	00000001	1941 R11	EQU	11
		0000000C	00000001	1942 R12	EQU	12
		0000000D	00000001	1943 R13	EQU	13
		0000000E	00000001	1944 R14	EQU	14
		0000000F	00000001	1945 R15	EQU	15
				1947	*****	
				1948	* Register equates	
				1949	*****	
		00000000	00000001	1951 V0	EQU	0
		00000001	00000001	1952 V1	EQU	1
		00000002	00000001	1953 V2	EQU	2
		00000003	00000001	1954 V3	EQU	3
		00000004	00000001	1955 V4	EQU	4
		00000005	00000001	1956 V5	EQU	5
		00000006	00000001	1957 V6	EQU	6
		00000007	00000001	1958 V7	EQU	7
		00000008	00000001	1959 V8	EQU	8
		00000009	00000001	1960 V9	EQU	9
		0000000A	00000001	1961 V10	EQU	10
		0000000B	00000001	1962 V11	EQU	11
		0000000C	00000001	1963 V12	EQU	12
		0000000D	00000001	1964 V13	EQU	13
		0000000E	00000001	1965 V14	EQU	14
		0000000F	00000001	1966 V15	EQU	15
		00000010	00000001	1967 V16	EQU	16
		00000011	00000001	1968 V17	EQU	17
		00000012	00000001	1969 V18	EQU	18
		00000013	00000001	1970 V19	EQU	19
		00000014	00000001	1971 V20	EQU	20
		00000015	00000001	1972 V21	EQU	21

[illegible]

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES														
BEGIN	I	00000200	2	156	122	152	153	154											
CTLR0	F	0000048C	4	351	166	167	168	169											
DECNUM	C	00001073	16	402	266	268	274	276											
E7TEST	4	00000000	64	416	215														
E7TESTS	F	00002AE0	4	1872	208														
EDIT	X	00001047	18	397	267	275													
ENDTEST	U	0000031E	1	252	213														
EOJ	I	00000470	4	341	201	255													
EOJPSW	D	00000460	8	339	341														
FAILCONT	U	0000030E	1	242															
FAILED	F	00001000	4	379	244	253													
FAILMSG	U	0000030A	1	236	226														
FAILPSW	D	00000478	8	343	345														
FAILTEST	I	00000488	4	345	256														
FB0001	F	00000280	8	185	189	190	192												
IMAGE	1	00000000	11168	0															
K	U	00000400	1	363	364	365	366												
K64	U	00010000	1	365															
M	U	00000007	1	420	273														
MB	U	00100000	1	366															
MSG	I	000003A8	4	301	200	284													
MSGCMD	C	000003F6	9	331	314	315													
MSGMSG	C	000003FF	95	332	308	329	306												
MSGMVC	I	000003F0	6	329	312														
MSGOK	I	000003BE	2	310	307														
MSGRET	I	000003DE	4	325	318	321													
MSGSAVE	F	000003E4	4	328	304	325													
NEXTE7	U	000002D4	1	210	229	247													
OPNAME	C	00000008	8	422	271														
PAGE	U	00001000	1	364															
PRT3	C	0000105D	18	400	267	268	269	275	276	277									
PRTLNE	C	00001008	16	385	392	283													
PRTLNG	U	0000003F	1	392	282														
PRTM	C	00001044	2	390	277														
PRTNAME	C	00001033	8	388	271														
PRTNUM	C	00001018	3	386	269														
R0	U	00000000	1	1930	116	166	169	189	191	192	193	198	217	218	243	244	281		
R1	U	00000001	1	1931	282	285	301	304	306	308	310	325							
					199	224	225	253	254	283	315	329	546	547	548	549	576		
					577	578	579	606	607	608	609	636	637	638	639	667	668		
					669	670	697	698	699	700	727	728	729	730	757	758	759		
					760	788	789	790	791	818	819	820	821	848	849	850	851		
					878	879	880	881	909	910	911	912	939	940	941	942	969		
					970	971	972	999	1000	1001	1002	1033	1034	1035	1036	1063	1064		
					1065	1066	1093	1094	1095	1096	1123	1124	1125	1126	1154	1155	1156		
					1157	1184	1185	1186	1187	1214	1215	1216	1217	1244	1245	1246	1247		
					1275	1276	1277	1278	1305	1306	1307	1308	1335	1336	1337	1338	1365		
					1366	1367	1368	1396	1397	1398	1399	1426	1427	1428	1429	1456	1457		
					1458	1459	1486	1487	1488	1489	1521	1522	1523	1524	1551	1552	1553		
					1554	1581	1582	1583	1584	1611	1612	1613	1614	1642	1643	1644	1645		
					1672	1673	1674	1675	1702	1703	1704	1705	1732	1733	1734	1735	1763		
					1764	1765	1766	1793	1794	1795	1796	1823	1824	1825	1826	1853	1854		
					1855	1856													
R10	U	0000000A	1	1940	154	163	164												
R11	U	0000000B	1	1941	221	222	552	582	612	642	673	703	733	763	794	824	854		
					884	915	945	975	1005	1039	1069	1099	1129	1160	1190	1220	1250		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE40	F	00002848	4	1739	1723	1724	1726	
RE41	F	000028E0	4	1770	1754	1755	1757	
RE42	F	00002978	4	1800	1784	1785	1787	
RE43	F	00002A10	4	1830	1814	1815	1817	
RE44	F	00002AA8	4	1860	1844	1845	1847	
RE5	F	00001380	4	674	658	659	661	
RE6	F	00001418	4	704	688	689	691	
RE7	F	000014B0	4	734	718	719	721	
RE8	F	00001548	4	764	748	749	751	
RE9	F	000015E0	4	795	779	780	782	
REA1	A	000010D4	4	540				
REA10	A	0000162C	4	812				
REA11	A	000016C4	4	842				
REA12	A	0000175C	4	872				
REA13	A	000017F4	4	903				
REA14	A	0000188C	4	933				
REA15	A	00001924	4	963				
REA16	A	000019BC	4	993				
REA17	A	00001A54	4	1027				
REA18	A	00001AEC	4	1057				
REA19	A	00001B84	4	1087				
REA2	A	0000116C	4	570				
REA20	A	00001C1C	4	1117				
REA21	A	00001CB4	4	1148				
REA22	A	00001D4C	4	1178				
REA23	A	00001DE4	4	1208				
REA24	A	00001E7C	4	1238				
REA25	A	00001F14	4	1269				
REA26	A	00001FAC	4	1299				
REA27	A	00002044	4	1329				
REA28	A	000020DC	4	1359				
REA29	A	00002174	4	1390				
REA3	A	00001204	4	600				
REA30	A	0000220C	4	1420				
REA31	A	000022A4	4	1450				
REA32	A	0000233C	4	1480				
REA33	A	000023D4	4	1515				
REA34	A	0000246C	4	1545				
REA35	A	00002504	4	1575				
REA36	A	0000259C	4	1605				
REA37	A	00002634	4	1636				
REA38	A	000026CC	4	1666				
REA39	A	00002764	4	1696				
REA4	A	0000129C	4	630				
REA40	A	000027FC	4	1726				
REA41	A	00002894	4	1757				
REA42	A	0000292C	4	1787				
REA43	A	000029C4	4	1817				
REA44	A	00002A5C	4	1847				
REA5	A	00001334	4	661				
REA6	A	000013CC	4	691				
REA7	A	00001464	4	721				
REA8	A	000014FC	4	751				
REA9	A	00001594	4	782				
READDR	A	0000001C	4	426	224			
REG2LOW	U	000000DD	1	369				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
REG2PATT	U	AABBCCDD	1	368			
RELEN	A	00000018	4	425			
RPTDWSAV	D	00000398	8	294	281	285	
RPTERROR	I	0000032C	4	262	237		
RPTSAVE	F	00000390	4	291	262	288	
RPTSVR5	F	00000394	4	292	263	287	
SKL0001	U	0000004E	1	182	198		
SKT0001	C	0000022A	20	179	182	199	
SVOLDPSW	U	00000140	0	118			
T1	A	000010B8	4	532	1875		
T10	A	00001610	4	804	1884		
T11	A	000016A8	4	834	1885		
T12	A	00001740	4	864	1886		
T13	A	000017D8	4	895	1887		
T14	A	00001870	4	925	1888		
T15	A	00001908	4	955	1889		
T16	A	000019A0	4	985	1890		
T17	A	00001A38	4	1019	1891		
T18	A	00001AD0	4	1049	1892		
T19	A	00001B68	4	1079	1893		
T2	A	00001150	4	562	1876		
T20	A	00001C00	4	1109	1894		
T21	A	00001C98	4	1140	1895		
T22	A	00001D30	4	1170	1896		
T23	A	00001DC8	4	1200	1897		
T24	A	00001E60	4	1230	1898		
T25	A	00001EF8	4	1261	1899		
T26	A	00001F90	4	1291	1900		
T27	A	00002028	4	1321	1901		
T28	A	000020C0	4	1351	1902		
T29	A	00002158	4	1382	1903		
T3	A	000011E8	4	592	1877		
T30	A	000021F0	4	1412	1904		
T31	A	00002288	4	1442	1905		
T32	A	00002320	4	1472	1906		
T33	A	000023B8	4	1507	1907		
T34	A	00002450	4	1537	1908		
T35	A	000024E8	4	1567	1909		
T36	A	00002580	4	1597	1910		
T37	A	00002618	4	1628	1911		
T38	A	000026B0	4	1658	1912		
T39	A	00002748	4	1688	1913		
T4	A	00001280	4	622	1878		
T40	A	000027E0	4	1718	1914		
T41	A	00002878	4	1749	1915		
T42	A	00002910	4	1779	1916		
T43	A	000029A8	4	1809	1917		
T44	A	00002A40	4	1839	1918		
T5	A	00001318	4	653	1879		
T6	A	000013B0	4	683	1880		
T7	A	00001448	4	713	1881		
T8	A	000014E0	4	743	1882		
T9	A	00001578	4	774	1883		
TESTING	F	00001004	4	380	218		
TNUM	H	00000004	2	418	217	265	
TSUB	A	00000000	4	417	221		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
TTABLE	F	00002AE0	4	1874	
V0	U	00000000	1	1951	
V1	U	00000001	1	1952	220
V10	U	0000000A	1	1961	
V11	U	0000000B	1	1962	
V12	U	0000000C	1	1963	
V13	U	0000000D	1	1964	
V14	U	0000000E	1	1965	
V15	U	0000000F	1	1966	
V16	U	00000010	1	1967	
V17	U	00000011	1	1968	
V18	U	00000012	1	1969	
V19	U	00000013	1	1970	
V1FUDGE	X	00001094	16	409	220
V101	X	000010E0	16	542	551
V1010	X	00001638	16	814	823
V1011	X	000016D0	16	844	853
V1012	X	00001768	16	874	883
V1013	X	00001800	16	905	914
V1014	X	00001898	16	935	944
V1015	X	00001930	16	965	974
V1016	X	000019C8	16	995	1004
V1017	X	00001A60	16	1029	1038
V1018	X	00001AF8	16	1059	1068
V1019	X	00001B90	16	1089	1098
V102	X	00001178	16	572	581
V1020	X	00001C28	16	1119	1128
V1021	X	00001CC0	16	1150	1159
V1022	X	00001D58	16	1180	1189
V1023	X	00001DF0	16	1210	1219
V1024	X	00001E88	16	1240	1249
V1025	X	00001F20	16	1271	1280
V1026	X	00001FB8	16	1301	1310
V1027	X	00002050	16	1331	1340
V1028	X	000020E8	16	1361	1370
V1029	X	00002180	16	1392	1401
V103	X	00001210	16	602	611
V1030	X	00002218	16	1422	1431
V1031	X	000022B0	16	1452	1461
V1032	X	00002348	16	1482	1491
V1033	X	000023E0	16	1517	1526
V1034	X	00002478	16	1547	1556
V1035	X	00002510	16	1577	1586
V1036	X	000025A8	16	1607	1616
V1037	X	00002640	16	1638	1647
V1038	X	000026D8	16	1668	1677
V1039	X	00002770	16	1698	1707
V104	X	000012A8	16	632	641
V1040	X	00002808	16	1728	1737
V1041	X	000028A0	16	1759	1768
V1042	X	00002938	16	1789	1798
V1043	X	000029D0	16	1819	1828
V1044	X	00002A68	16	1849	1858
V105	X	00001340	16	663	672
V106	X	000013D8	16	693	702
V107	X	00001470	16	723	732

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	11168	0000- 2B9F	0000- 2B9F
Regi on		11168	0000- 2B9F	0000- 2B9F
CSECT	ZVE7TST	11168	0000- 2B9F	0000- 2B9F

```
1 /home/tn529/sharedvfp/tests/zvector-e7-14-MergePack.asm
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**** NO ERRORS FOUND ****