

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction performance tests for 64 instructions
				5 *
				6 * James Wekel May 2025
				7 *****
				8
				9 *****
				10 *
				11 * Example Hercules Testcase:
				12 *
				13 * *Testcase zvector-e7-99-performance
				14 *
				15 * # -----
				16 * # This ONLY tests the performance of the Zvector instructions.
				17 * #
				18 * # The default is to NOT run performance tests. To enable
				19 * # performance tests, uncomment the "#r 500=ff" line
				20 * # below and swap the runtest commands.
				21 * #
				22 * # The default test is 30,000,000 iterations of the zvector
				23 * # instruction. The iteration count can be modified at address 504.
				24 * # For example, "r 504=01312D00" would set the
				25 * # iteration count to 20,000,000.
				26 * #
				27 * # Tests: 64 E7 zvector instructions
				28 * #
				29 * # Output:
				30 * # For each test, a console line will be generated with timing
				31 * # results, as follows:
				32 * #
				33 * # Test # 001: 30,000,000 iterations of "VLREPB V1,0(R5)"
				34 * # took 503,528 microseconds
				35 * # Test # 002: 30,000,000 iterations of "VESL V1,V2,3,0"
				36 * # took 145,584 microseconds
				37 * # Test # 003: 30,000,000 iterations of "VERLL V1,V2,3,0"
				38 * # took 163,143 microseconds
				39 * # Test # 004: 30,000,000 iterations of "VESRL V1,V2,3,0"
				40 * # took 138,747 microseconds
				41 * # Test # 005: 30,000,000 iterations of "VESRA V1,V2,3,0"
				42 * # took 153,151 microseconds
				43 * # ...
				44 * #
				45 * # Note:
				46 * # this test requires diagnose 'F14' for OS microsecond timing.
				47 * # -----
				48 * mainsize 2
				49 * numcpu 1
				50 * sysclear
				51 * archlvl z/Arch
				52 * diag8cmd enable # (needed for messages to Hercules console)
				53 *
				54 * loadcore "\$(testpath)/zvector-e7-99-performance.core" 0x0
				55 *
				56 * #r 500=ff # (enable timing tests)
				57 * #r 504=01312D00 # (20,000,000 iteration count for test)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
66				*****
67	*			FCHECK Macro - Is a Facility Bit set?
68	*			
69	*			If the facility bit is NOT set, an message is issued and
70	*			the test is skipped.
71	*			
72	*			Fcheck uses R0, R1 and R2
73	*			
74	* eg.			FCHECK 134, 'vector-packed-decimal'
75	*****			*****
76				MACRO
77				FCHECK &BITNO, &NOTSETMSG
78	. *			&BITNO : facility bit number to check
79	. *			&NOTSETMSG : 'facility name'
80		LCLA	&FBBYTE	Facility bit in Byte
81		LCLA	&FBBIT	Facility bit within Byte
82				
83		LCLA	&L(8)	
84	&L(1)	SetA	128, 64, 32, 16, 8, 4, 2, 1	bit positions within byte
85				
86	&FBBYTE	SETA	&BITNO/8	
87	&FBBIT	SETA	&L((&BITNO-(&FBBYTE*8))+1)	
88	. *	MNOTE	0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'	
89				
90		B	X&SYSNDX	
91	*			Fcheck data area
92	*			skip messgae
93	SKT&SYSNDX DC	C'	Skipping tests: '	
94		DC	C&NOTSETMSG	
95		DC	C' (bit &BITNO) is not installed.'	
96	SKL&SYSNDX EQU	*	- SKT&SYSNDX	
97	*			facility bits
98		DS	FD	gap
99	FB&SYSNDX DS	4FD		
100		DS	FD	gap
101	*			
102	X&SYSNDX EQU *			
103		LA	R0, ((X&SYSNDX- FB&SYSNDX)/8)-1	
104		STFLE	FB&SYSNDX	get facility bits
105				
106		XGR	R0, R0	
107		IC	R0, FB&SYSNDX+&FBBYTE	get fbit byte
108		N	R0, =F' &FBBIT'	is bit set?
109		BNZ	XC&SYSNDX	
110	*			
111	*			facility bit not set, issue message and exit
112	*			
113		LA	R0, SKL&SYSNDX	message length
114		LA	R1, SKT&SYSNDX	message address
115		BAL	R2, MSG	
116				
117		B	EOJ	
118	XC&SYSNDX EQU *			
119			MEND	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				139	*****
				140	* The actual "ZVE7TST" program itself...
				141	*****
				142	*
				143	* Architecture Mode: z/Arch
				144	* Register Usage:
				145	*
				146	* R0 (work)
				147	* R1-4 (work)
				148	* R5 Testing control table - current test base
				149	* R6- R7 (work)
				150	* R8 First base register
				151	* R9 Second base register
				152	* R10 Third base register
				153	* R11 E7TEST call return
				154	* R12 E7TESTS register
				155	* R13 (work)
				156	* R14 Subroutine call
				157	* R15 Secondary Subroutine call or work
				158	*
				159	*****
00000200		00000200		161	USING BEGIN, R8 FIRST Base Register
00000200		00001200		162	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		163	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			165	BEGIN BALR R8, 0 Initalize FIRST base register
00000202	0680			166	BCTR R8, 0 Initalize FIRST base register
00000204	0680			167	BCTR R8, 0 Initalize FIRST base register
00000206	4190 8800		00000800	169	LA R9, 2048(, R8) Initalize SECOND base register
0000020A	4190 9800		00000800	170	LA R9, 2048(, R9) Initalize SECOND base register
				171	
0000020E	41A0 9800		00000800	172	LA R10, 2048(, R9) Initalize THIRD base register
00000212	41A0 A800		00000800	173	LA R10, 2048(, R10) Initalize THIRD base register
				174	
00000216	95FF 8400		00000600	175	CLI TIMEOPT, X' FF' Is this a timing run?
0000021A	4770 8760		00000960	176	BNE EOJ Not a timing run; just end normally
				177	
0000021E	B600 877C		0000097C	178	STCTL R0, R0, CTLR0 Store CRO to enable AFP
00000222	9604 877D		0000097D	179	OI CTLR0+1, X' 04' Turn on AFP bit
00000226	9602 877D		0000097D	180	OI CTLR0+1, X' 02' Turn on Vector bit
0000022A	B700 877C		0000097C	181	LCTL R0, R0, CTLR0 Reload updated CRO

[illegible]

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				316 *	
				317 **	Run the performance tests...
				318 *	
000004E0				319 D0TEST	DS 0F
000004E0	45E0 8528		00000728	320	BAL R14, TEST91 Time instructions (speed test)
				321	
				322	*****
				323 *	Test for normal or unexpected test completion...
				324	*****
				325	
000004E4	95FF 8400		00000600	326	CLI TIMEOPT, X' FF' Was this a timing run?
000004E8	4770 8760		00000960	327	BNE E0J No, timing run; just go end normally
				328	
000004EC	5810 8794		00000994	329	L R1, =A(TTBLNUM) Get number of tests
000004F0	5811 0000		00000000	330	L R1, 0(R1)
				331	
000004F4	5820 840C		0000060C	332	L R2, TESTING
000004F8	1912			333	CR R1, R2 Did we end on last performance test?
000004FA	4770 8778		00000978	334	BNE FAILTEST No?! Then FAIL the test!
				335	
000004FE	47F0 8760		00000960	336	B E0J Yes, then normal completion!
				338	*****
				339 *	Fixed test storage locations ...
				340	*****
00000502		00000502	00000600	342	ORG BEGIN+X' 400'
				343	
00000600	00			344 TIMEOPT	DC X' 00' Set to non-zero to run timing tests
00000601	00			345	DC X' 00' gap
00000604	01C9C380			346 ITERCNT	DC F' 30000000' instruction test iterations
				347 *	
00000608	00000000			348 FAILED	DC F' 0' some test failed?
0000060C	00000000			349 TESTING	DC F' 0' current test number
				350	
00000610				352	DS 0D
00000610	00000000 00000000			353 SAVE3T5	DC 4F' 0'
00000620	00000000			354 SAVER2	DC F' 0'
00000624	00000000			355 SAVER5	DC F' 0'
				356	
00000628		00000628	00000728	358	ORG *+X' 100'

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT	
					360	*****
					361	* TEST91 Time zvector instruction (speed test)
					362	*****
					363	
00000728					364	TEST91 DS OF
00000728	58C0	8798		00000998	365	L R12, =A(E7TESTS) get table of test addresses
					366	
					367	*****
					368	* Next, time the tests...
					369	*****
					370	
			0000072C	00000001	371	NEXTE7 EQU *
0000072C	5850	C000		00000000	372	L R5, 0(0, R12) get test address
00000730	1255				373	LTR R5, R5 have a test?
00000732	078E				374	BZR R14 done?
					375	
00000734				00000000	376	USING E7TEST, R5
					377	
00000734	4800	5004		00000004	378	LH R0, TNUM save current test number
00000738	5000	840C		0000060C	379	ST R0, TESTING for easy reference
					380	*
					381	* Initialize operand data (move source to testing address)
					382	*
0000073C	E310	5014	0014	00000014	383	LGF R1, V2ADDR load v2 source
00000742	E721	0000	0006	00000000	384	VL v2, 0(R1)
					385	
00000748	E310	5018	0014	00000018	386	LGF R1, V3ADDR load v3 source
0000074E	E731	0000	0006	00000000	387	VL v3, 0(R1)
					388	
00000754	E310	501C	0014	0000001C	389	LGF R1, V4ADDR load v4 source
0000075A	E741	0000	0006	00000000	390	VL v4, 0(R1)
					391	
					392	*****
					393	* Time the overhead...
					394	*****
00000760	5870	8404		00000604	395	L R7, ITERCNT
					396	
00000764	83120F14				397	DC X' 83' , X' 12' , X' 0F14' Issue Hercules Diagnose X' F14'
00000768	E310	87A8	0024	000009A8	398	STG R1, MSBEGCLK
					399	
			0000076E	00000001	400	OHL00P EQU *
0000076E	4670	856E		0000076E	401	BCT R7, OHL00P
					402	
00000772	83120F14				403	DC X' 83' , X' 12' , X' 0F14' Issue Hercules Diagnose X' F14'
00000776	E310	87B0	0024	000009B0	404	STG R1, MSENDCLK
					405	
0000077C	E310	87A8	0009	000009A8	406	SG R1, MSBEGCLK
00000782	E310	87A0	0024	000009A0	407	STG R1, MSOVER

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				440	*****			
				441	*	RPTSPEED	Report instruction speed	
				442	*****			
000007CC	50F0 8654		00000854	444	RPTSPEED	ST	R15, RPTSAVE	Save return address
000007D0	905D 8670		00000870	445		STM	R5, R13, R5AV5T13	Save R5 to R13
				446	*			
000007D4	5820 840C		0000060C	447		L	R2, TESTING	get test number and convert
000007D8	4E20 88C2		00000AC2	448		CVD	R2, DECNUM	
000007DC	D20F 884C 8834	00000A4C	00000A34	449		MVC	PTNUM, EDITTNUM	
000007E2	DE0F 884C 88C2	00000A4C	00000AC2	450		ED	PTNUM, DECNUM	
000007E8	D202 87E0 8859	000009E0	00000A59	451		MVC	PRTNUM(3), PTNUM+L' PTNUM-3	fill in message with test #
				452				
000007EE	5820 8404		00000604	453		L	R2, ITERCNT	get iteration count
000007F2	4E20 88C2		00000AC2	454		CVD	R2, DECNUM	
000007F6	D211 887C 8860	00000A7C	00000A60	455		MVC	PITER, EDITITER	
000007FC	DE11 887C 88C2	00000A7C	00000AC2	456		ED	PITER, DECNUM	
00000802	D209 87E5 8884	000009E5	00000A84	457		MVC	PRTITR(10), PITER+L' PITER-10	fill in iteration count
				458				
00000808	5820 500C		0000000C	459		L	R2, CMTADDR	
0000080C	D217 87FE 2000	000009FE	00000000	460		MVC	PRTCMT(24), 0(R2)	
				461	*			
				462				
00000812	E310 87B8 0004		000009B8	463		LG	R1, MSDUR	
00000818	E310 87A0 0009		000009A0	464		SG	R1, MSOVER	
0000081E	4E10 87D0		000009D0	465		CVD	R1, MSAAA	
				466				
00000822	D211 88AC 8892	00000AAC	00000A92	467		MVC	PMS, EDITMS	
00000828	DE11 88AC 87D0	00000AAC	000009D0	468		ED	PMS, MSAAA	
0000082E	D20A 881C 88B3	00000A1C	00000AB3	469		MVC	PRTMS(L' PRTMS), PMS+L' PMS- L' PRTMS	
				471	*			
				472	*			
				473	*			
00000834	9002 8660		00000860	474		STM	R0, R2, RPTDWSAV	save regs used by MSG
00000838	4100 005C		0000005C	475		LA	R0, PRTLNG	message length
0000083C	4110 87D8		000009D8	476		LA	R1, PRTLNE	messagfe address
00000840	4520 8698		00000898	477		BAL	R2, MSG	call console MSG display
00000844	9802 8660		00000860	478		LM	R0, R2, RPTDWSAV	restore regs
				480				
00000848	985D 8670		00000870	480		LM	R5, R13, R5AV5T13	
0000084C	58F0 8654		00000854	481		L	R15, RPTSAVE	Restore return address
00000850	07FF			482		BR	R15	Return to caller
				484	RPTSAVE	DC	F' 0'	R15 save area
00000854	00000000			485	RPTSVR5	DC	F' 0'	R5 save area
00000858	00000000							
00000860	00000000 00000000			487	RPTDWSAV	DC	2D' 0'	R0-R2 save area for MSG call
00000870	00000000 00000000			488	R5AV5T13	DC	10F' 0'	

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT			
					536	*****		
					537	* Working Storage		
					538	*****		
0000097C	00000000				540	CTLRO	DS	F CRO
					541			
00000980					543	LTORG		Literals pool
00000980	FFFFFFFF	FFFFFFFF			544			=D' - 1'
00000988	00000040				545			=F' 64'
0000098C	00000001				546			=F' 1'
00000990	00000008				547			=F' 8'
00000994	00002808				548			=A(TTBLNUM)
00000998	00002700				549			=A(E7TESTS)
0000099C	0000				550			=H' 0'
0000099E	005F				551			=AL2(L' MSGMSG)
			00000400	00000001	553	K	EQU	1024 One KB
			00001000	00000001	554	PAGE	EQU	(4*K) Size of one page
			00004000	00000001	555	K16	EQU	(16*K) 16 KB
			00008000	00000001	556	K32	EQU	(32*K) 32 KB
			00010000	00000001	557	K64	EQU	(64*K) 64 KB
			00100000	00000001	558	MB	EQU	(K*K) 1 MB
					560			
000009A0	00000000	00000000			561	MSOVER	DC	D' 0' MS Overhead
000009A8	00000000	00000000			562	MSBEGCLK	DC	D' 0' MS Begin
000009B0	00000000	00000000			563	MSENDCLK	DC	D' 0' MS End
000009B8	00000000	00000000			564	MSDUR	DC	D' 0' MS Duration (diff)
000009C0	00000000	00000000			565		DC	D' 0' , 8X' AA' gap
000009D0	00000000	0000000C			566	MSAAA	DC	PL8' 0' MS packed
					567			
000009D8	40E385A2	A3407B40			568	PRTLIN	DC	C' Test # '
000009E0	A7A7A7				569	PRTNUM	DC	C' xxx'
000009E3	7A40				570		DC	C' : '
000009E5	F9F96BF9	F9F96BF9			571	PRTITR	DC	C' 99, 999, 999'
000009EF	4089A385	9981A389			572		DC	C' iterations of '
000009FE	40404040	40404040			573	PRTCMT	DC	CL24' '
00000A16	40A39696	9240			574		DC	C' took '
00000A1C	F9F9F96B	F9F9F96B			575	PRTMS	DC	C' 999, 999, 999'
00000A27	40948983	9996A285			576		DC	C' microseconds'
			0000005C	00000001	577	PRTLNG	EQU	* - PRTLIN
					578	*		
					579	* edit fields for message line		
					580	*		
00000A34	40212020	20202020			581	EDITTNUM	DC	XL16' 402120202020202020202020202020'
00000A48					582		DS	0D
00000A48	7E7E7E6E				583		DC	C' ==>'
00000A4C	40404040	40404040			584	PTNUM	DC	CL16' '
00000A5C	4C7E7E7E				585		DC	C' <==>'
					586			
00000A60	40202020	20202020			587	EDITITER	DC	XL18' 40202020202020202020206B2020206B202120'
00000A78					588		DS	0D
00000A78	7E7E7E6E				589		DC	C' ==>'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				604 ***** 605 * E7TEST DSECT 606 *****
00000000	00000000			608 E7TEST DSECT , 609 TSUB DC A(0) pointer to test 00000004 0000 610 TNUM DC H' 00' Test Number 00000006 0000 611 DC H' 00' 00000008 0000 612 LCMF DC H' 00' length of comment 0000000C 00000000 613 CMTADDR DC A(0) address of comment 00000010 00000000 614 INADDR DC A(0) address of instruction under test 00000014 00000000 615 V2ADDR DC A(0) address of v2 source 00000018 00000000 616 V3ADDR DC A(0) address of v3 source 0000001C 00000000 617 V4ADDR DC A(0) address of v4 source 618 619 620 * test routine will be here 621 * 622 * followed by 623 * EXPECTED RESULT
00000AEC		00000000	0000280F	625 ZVE7TST CSECT , 626 DS OF

LOC	OBJECT	CODE	ADDR1	ADDR2	STMT
					628 *****
					629 * Macros to help build test tables
					630 *****
					631
					632 * -----
					633 * PTEST: macro to generate individual test
					634 * -----
					635 MACRO
					636 PTEST &CMT
					637 . * &CMT - messgae comment to identify
					638 . * test
					639 GBLA &TNUM
					640 &TNUM SETA &TNUM+1
					641
					642 &C SETC ' &CMT'
					643 &LCMT SETA K' &C
					644
					645 DS OFD
					646 USING *, R5 base for test data and test routine
					647
					648 T&TNUM DC A(X&TNUM) address of test routine
					649 DC H' &TNUM test number
					650 DC H' 00'
					651
					652 DC H' &LCMT' length of comment
					653 DC A(CMT&TNUM) address of comment
					654 DC A(IN&TNUM) address of instruction
					655 DC A(IN&TNUM+6) address of v2 source
					656 DC A(IN&TNUM+22) address of v3 source
					657 DC A(IN&TNUM+38) address of v4
					658 . *
					659 *
					660 X&TNUM DS OF
					661 . *
					662 CMT&TNUM DC CL24&C
					663 . * is comment longer than 24 charaters
					664 AIF (&LCMT LE 26).SKWN note: length includes enclosing 's
					665 MNOTE 4, 'Comment truncated to 24 characters'
					666 . SKWN ANOP
					667
					668 IN&TNUM DC OF zvector instruction for performance test
					669
					670 DROP R5
					671 MEND

673	*	-----	
674	*	PTTABLE: macro to generate table of pointers to individual tests	
675	*	-----	
676		MACRO	
677		PTTABLE	
678		GBLA	&TNUM
679		LCLA	&CUR
680	&CUR	SETA	1
681	. *		
682	TTABLE	DS	OF
683	. LOOP	ANOP	
684	. *		
685		DC	A(T&CUR)
686	. *		
687	&CUR	SETA	&CUR+1
688		AIF	(&CUR LE &TNUM) . LOOP
689	*		
690		DC	A(0) END OF TABLE
691		DC	A(0)
692			
693	TTBLNUM	DC	F' &TNUM
694		DC	A(0)
695	. *		
696		MEND	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				698 *****
				699 * Performance tests
				700 *****
00000AF0	00000000 00000000			701 PRINT DATA
				702 DS FD
				703 *
				704 * PTEST comment
				705 * followed by
				706 * 6 byte vector instruction to test performance
				707 * 16 byte V2 source
				708 * 16 byte V3 source
				709 * 16 byte V4 source
				710
				711 *-----
				712 * E705 VLREP - Vector Load and Replicate
				713 *-----
				714
00000AF8				715 PTEST ' "VLREPB V1, 0(R5) "'
00000AF8		00000AF8		716+ DS OFD
00000AF8	00000B18			717+ USING *, R5 base for test data and test routine
00000AFC	0001			718+T1 DC A(X1) address of test routine
00000AFE	0000			719+ DC H' 1' test number
00000B00	0013			720+ DC H' 00'
00000B04	00000B18			721+ DC H' 19' length of comment
00000B08	00000B30			722+ DC A(CMT1) address of comment
00000B0C	00000B36			723+ DC A(IN1) address of instruction
00000B10	00000B46			724+ DC A(IN1+6) address of v2 source
00000B14	00000B56			725+ DC A(IN1+22) address of v3 source
				726+ DC A(IN1+38) address of v4
				727+*
00000B18				728+X1 DS OF
00000B18	7FE5D3D9 C5D7C240			729+CMT1 DC CL24' "VLREPB V1, 0(R5) "'
00000B20	E5F16BF0 4DD9F55D			
00000B28	7F404040 40404040			
00000B30				730+IN1 DC OF zvector instruction for performance test
00000B30				731+ DROP R5
00000B30	E715 0000 0005	00000000		732 VLREPB V1, 0(R5)
00000B36	AAAAAAAA AAAAAAAAAA			733 DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA' v2
00000B3E	AAAAAAAA AAAAAAAAAA			
00000B46	AABBBBAA AABBAAAA			734 DC XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA' v3
00000B4E	BBAAAABB AAAABBA			
00000B56	00000000 00000002			735 DC XL16' 0000000000000002 0000000000000000' v4
00000B5E	00000000 00000000			
				736
				737 *-----
				738 * E730 VESL - Vector Element Shift Left
				739 *-----
				740
00000B68				741 PTEST ' "VESL V1, V2, 3, 0"'
00000B68		00000B68		742+ DS OFD
00000B68	00000B88			743+ USING *, R5 base for test data and test routine
00000B6C	0002			744+T2 DC A(X2) address of test routine
00000B6E	0000			745+ DC H' 2' test number
00000B70	0014			746+ DC H' 00'
00000B74	00000B88			747+ DC H' 20' length of comment
				748+ DC A(CMT2) address of comment

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00000B78	00000BA0			749+	DC	A(IN2)	address of instruction
00000B7C	00000BA6			750+	DC	A(IN2+6)	address of v2 source
00000B80	00000BB6			751+	DC	A(IN2+22)	address of v3 source
00000B84	00000BC6			752+	DC	A(IN2+38)	address of v4
				753+*			
00000B88				754+X2	DS	0F	
00000B88	7FE5C5E2 D3404040			755+CMF2	DC	CL24' "VESL V1, V2, 3, 0"	
00000B90	E5F16BE5 F26BF36B						
00000B98	F07F4040 40404040						
00000BA0				756+IN2	DC	0F	zvector instruction for performance test
00000BA0				757+	DROP	R5	
00000BA0	E712 0003 0030		00000003	758	VESL	V1, V2, 3, 0	
00000BA6	AAAAAAAA AAAAAAAAAA			759	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
00000BAE	AAAAAAAA AAAAAAAAAA						
00000BB6	AABBBBAA AABBAAAA			760	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAAAABBAA'	v3
00000BBE	BBAAAABB AAAABBAA						
00000BC6	00000000 00000002			761	DC	XL16' 0000000000000002 0000000000000000'	v4
00000BCE	00000000 00000000						
				762			
				763 *			
				764 *	E733 VERLL	- Vector Element Rotate Left Logical	
				765 *			
				766			
				767	PTEST	' "VERLL V1, V2, 3, 0"	
00000BD8				768+	DS	0FD	
00000BD8		00000BD8		769+	USING	*, R5	base for test data and test routine
00000BD8	00000BF8			770+T3	DC	A(X3)	address of test routine
00000BDC	0003			771+	DC	H' 3'	test number
00000BDE	0000			772+	DC	H' 00'	
00000BE0	0014			773+	DC	H' 20'	length of comment
00000BE4	00000BF8			774+	DC	A(CMF3)	address of comment
00000BE8	00000C10			775+	DC	A(IN3)	address of instruction
00000BEC	00000C16			776+	DC	A(IN3+6)	address of v2 source
00000BF0	00000C26			777+	DC	A(IN3+22)	address of v3 source
00000BF4	00000C36			778+	DC	A(IN3+38)	address of v4
				779+*			
00000BF8				780+X3	DS	0F	
00000BF8	7FE5C5D9 D3D34040			781+CMF3	DC	CL24' "VERLL V1, V2, 3, 0"	
00000C00	E5F16BE5 F26BF36B						
00000C08	F07F4040 40404040						
00000C10				782+IN3	DC	0F	zvector instruction for performance test
00000C10				783+	DROP	R5	
00000C10	E712 0003 0033		00000003	784	VERLL	V1, V2, 3, 0	
00000C16	AAAAAAAA AAAAAAAAAA			785	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
00000C1E	AAAAAAAA AAAAAAAAAA						
00000C26	AABBBBAA AABBAAAA			786	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAAAABBAA'	v3
00000C2E	BBAAAABB AAAABBAA						
00000C36	00000000 00000002			787	DC	XL16' 0000000000000002 0000000000000000'	v4
00000C3E	00000000 00000000						
				788			
				789 *			
				790 *	E738 VESRL	- Vector Element Shift Right Logical	
				791 *			
				792			
				793	PTEST	' "VESRL V1, V2, 3, 0"	
00000C48				794+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00000C48		00000C48		795+	USING *, R5	base for test data and test routine
00000C48	00000C68			796+T4	DC A(X4)	address of test routine
00000C4C	0004			797+	DC H' 4'	test number
00000C4E	0000			798+	DC H' 00'	
00000C50	0014			799+	DC H' 20'	length of comment
00000C54	00000C68			800+	DC A(CMT4)	address of comment
00000C58	00000C80			801+	DC A(IN4)	address of instruction
00000C5C	00000C86			802+	DC A(IN4+6)	address of v2 source
00000C60	00000C96			803+	DC A(IN4+22)	address of v3 source
00000C64	00000CA6			804+	DC A(IN4+38)	address of v4
				805+*		
00000C68				806+X4	DS 0F	
00000C68	7FE5C5E2 D9D34040			807+CMT4	DC CL24' "VESRL V1, V2, 3, 0"	
00000C70	E5F16BE5 F26BF36B					
00000C78	F07F4040 40404040					
00000C80				808+IN4	DC 0F	zvector instruction for performance test
00000C80				809+	DROP R5	
00000C80	E712 0003 0038		00000003	810	VESRL V1, V2, 3, 0	
00000C86	AAAAAAAA AAAAAAAAAA			811	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
00000C8E	AAAAAAAA AAAAAAAAAA					
00000C96	AABBBBAA AABBAAAA			812	DC XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA'	v3
00000C9E	BBAAAABB AAAABBA					
00000CA6	00000000 00000002			813	DC XL16' 0000000000000002 0000000000000000'	v4
00000CAE	00000000 00000000					
				814		
				815 *	-----	
				816 *	E73A VESRA - Vector Element Shift Right Arithmetic	
				817 *	-----	
				818		
00000CB8				819	PTEST ' "VESRA V1, V2, 3, 0"	
00000CB8		00000CB8		820+	DS 0FD	
00000CB8	00000CD8			821+	USING *, R5	base for test data and test routine
00000CBC	0005			822+T5	DC A(X5)	address of test routine
00000CBE	0000			823+	DC H' 5'	test number
00000CC0	0014			824+	DC H' 00'	
00000CC4	00000CD8			825+	DC H' 20'	length of comment
00000CC8	00000CF0			826+	DC A(CMT5)	address of comment
00000CCC	00000CF6			827+	DC A(IN5)	address of instruction
00000CD0	00000D06			828+	DC A(IN5+6)	address of v2 source
00000CD4	00000D16			829+	DC A(IN5+22)	address of v3 source
				830+	DC A(IN5+38)	address of v4
				831+*		
00000CD8				832+X5	DS 0F	
00000CD8	7FE5C5E2 D9C14040			833+CMT5	DC CL24' "VESRA V1, V2, 3, 0"	
00000CE0	E5F16BE5 F26BF36B					
00000CE8	F07F4040 40404040					
00000CF0				834+IN5	DC 0F	zvector instruction for performance test
00000CF0				835+	DROP R5	
00000CF0	E712 0003 003A		00000003	836	VESRA V1, V2, 3, 0	
00000CF6	AAAAAAAA AAAAAAAAAA			837	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
00000CFE	AAAAAAAA AAAAAAAAAA					
00000D06	AABBBBAA AABBAAAA			838	DC XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA'	v3
00000D0E	BBAAAABB AAAABBA					
00000D16	00000000 00000002			839	DC XL16' 0000000000000002 0000000000000000'	v4
00000D1E	00000000 00000000					
				840		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				841 *	-----
				842 *	E744 VGBM - Vector Generate Byte Mask
				843 *	-----
				844	
				845	PTEST ' "VGBM V1, 170"'
00000D28				846+	DS OFD
00000D28		00000D28		847+	USING *, R5
00000D28	00000D48			848+T6	DC A(X6)
00000D2C	0006			849+	DC H' 6'
00000D2E	0000			850+	DC H' 00'
00000D30	0011			851+	DC H' 17'
00000D34	00000D48			852+	DC A(CMT6)
00000D38	00000D60			853+	DC A(IN6)
00000D3C	00000D66			854+	DC A(IN6+6)
00000D40	00000D76			855+	DC A(IN6+22)
00000D44	00000D86			856+	DC A(IN6+38)
				857+*	
00000D48				858+X6	DS OF
00000D48	7FE5C7C2 D4404040			859+CMT6	DC CL24' "VGBM V1, 170"'
00000D50	E5F16BF1 F7F07F40				
00000D58	40404040 40404040				
00000D60				860+IN6	DC OF
00000D60				861+	DROP R5
00000D60	E710 00AA 0044			862	VGBM V1, 170
00000D66	AAAAAAAA AAAAAAAAAA			863	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA' v2
00000D6E	AAAAAAAA AAAAAAAAAA				
00000D76	AABBBBAA AABBAAAA			864	DC XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA' v3
00000D7E	BBAAAABB AAAABBA				
00000D86	00000000 00000002			865	DC XL16' 0000000000000002 0000000000000000' v4
00000D8E	00000000 00000000				
				866	
				867 *	-----
				868 *	E745 VREPI - Vector Replicate Immediate
				869 *	-----
				870	
				871	PTEST ' "VREPI V1, 170, 0"'
00000D98				872+	DS OFD
00000D98		00000D98		873+	USING *, R5
00000D98	00000DB8			874+T7	DC A(X7)
00000D9C	0007			875+	DC H' 7'
00000D9E	0000			876+	DC H' 00'
00000DA0	0013			877+	DC H' 19'
00000DA4	00000DB8			878+	DC A(CMT7)
00000DA8	00000DD0			879+	DC A(IN7)
00000DAC	00000DD6			880+	DC A(IN7+6)
00000DB0	00000DE6			881+	DC A(IN7+22)
00000DB4	00000DF6			882+	DC A(IN7+38)
				883+*	
00000DB8				884+X7	DS OF
00000DB8	7FE5D9C5 D7C94040			885+CMT7	DC CL24' "VREPI V1, 170, 0"'
00000DC0	E5F16BF1 F7F06BF0				
00000DC8	7F404040 40404040				
00000DD0				886+IN7	DC OF
00000DD0				887+	DROP R5
00000DD0	E710 00AA 0045			888	VREPI V1, 170, 0
00000DD6	AAAAAAAA AAAAAAAAAA			889	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA' v2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00000DDE	AAAAAAAA AAAAAAAAAA						
00000DE6	AABBBBAA AABBAAAA			890	DC	XL16' AABBBBAAAAABBAAAA BBAAAABBAABBAABBA'	v3
00000DEE	BBAAAABB AAAABBA						
00000DF6	00000000 00000002			891	DC	XL16' 00000000000000002 0000000000000000'	v4
00000DFE	00000000 00000000						
				892			
				893	*	-----	
				894	*	E746 VGM - Vector Generate Mask	
				895	*	-----	
				896			
				897	PTEST	' "VGM V1, 2, 4, 0"'	
00000E08				898+	DS	OFD	
00000E08		00000E08		899+	USING	*, R5	base for test data and test routine
00000E08	00000E28			900+T8	DC	A(X8)	address of test routine
00000E0C	0008			901+	DC	H' 8'	test number
00000E0E	0000			902+	DC	H' 00'	
00000E10	0013			903+	DC	H' 19'	length of comment
00000E14	00000E28			904+	DC	A(CMT8)	address of comment
00000E18	00000E40			905+	DC	A(IN8)	address of instruction
00000E1C	00000E46			906+	DC	A(IN8+6)	address of v2 source
00000E20	00000E56			907+	DC	A(IN8+22)	address of v3 source
00000E24	00000E66			908+	DC	A(IN8+38)	address of v4
				909+*			
00000E28				910+X8	DS	OF	
00000E28	7FE5C7D4 40404040			911+CMT8	DC	CL24' "VGM V1, 2, 4, 0"'	
00000E30	E5F16BF2 6BF46BF0						
00000E38	7F404040 40404040						
00000E40				912+IN8	DC	OF	zvector instruction for performance test
00000E40				913+	DROP	R5	
00000E40	E710 0204 0046			914	VGM	V1, 2, 4, 0	
00000E46	AAAAAAAA AAAAAAAAAA			915	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
00000E4E	AAAAAAAA AAAAAAAAAA						
00000E56	AABBBBAA AABBAAAA			916	DC	XL16' AABBBBAAAAABBAAAA BBAAAABBAABBAABBA'	v3
00000E5E	BBAAAABB AAAABBA						
00000E66	00000000 00000002			917	DC	XL16' 00000000000000002 0000000000000000'	v4
00000E6E	00000000 00000000						
				918			
				919	*	-----	
				920	*	E74D VREP - Vector Replicate	
				921	*	-----	
				922			
				923	PTEST	' "VREP V1, V2, 4, 0"'	
00000E78				924+	DS	OFD	
00000E78		00000E78		925+	USING	*, R5	base for test data and test routine
00000E78	00000E98			926+T9	DC	A(X9)	address of test routine
00000E7C	0009			927+	DC	H' 9'	test number
00000E7E	0000			928+	DC	H' 00'	
00000E80	0014			929+	DC	H' 20'	length of comment
00000E84	00000E98			930+	DC	A(CMT9)	address of comment
00000E88	00000EB0			931+	DC	A(IN9)	address of instruction
00000E8C	00000EB6			932+	DC	A(IN9+6)	address of v2 source
00000E90	00000EC6			933+	DC	A(IN9+22)	address of v3 source
00000E94	00000ED6			934+	DC	A(IN9+38)	address of v4
				935+*			
00000E98				936+X9	DS	OF	
00000E98	7FE5D9C5 D7404040			937+CMT9	DC	CL24' "VREP V1, V2, 4, 0"'	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00000EA0	E5F16BE5 F26BF46B					
00000EA8	F07F4040 40404040					
00000EB0				938+IN9	DC 0F	zvector instruction for performance test
00000EB0				939+	DROP R5	
00000EB0	E712 0004 004D			940	VREP V1, V2, 4, 0	
00000EB6	AAAAAAAA AAAAAAAAAA			941	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
00000EBE	AAAAAAAA AAAAAAAAAA					
00000EC6	AABBBBAA AABBAAAA			942	DC XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA'	v3
00000ECE	BBAAAABB AAAABBA					
00000ED6	00000000 00000002			943	DC XL16' 0000000000000002 0000000000000000'	v4
00000EDE	00000000 00000000					
				944		
				945 *	-----	
				946 *	E75C VISTR - Vector Isolate String	
				947 *	-----	
				948		
				949	PTEST ' "VISTR V1, V2, 0"'	
00000EE8				950+	DS OFD	
00000EE8		00000EE8		951+	USING *, R5	base for test data and test routine
00000EE8	00000F08			952+T10	DC A(X10)	address of test routine
00000EEC	000A			953+	DC H' 10'	test number
00000EEE	0000			954+	DC H' 00'	
00000EF0	0012			955+	DC H' 18'	length of comment
00000EF4	00000F08			956+	DC A(CMT10)	address of comment
00000EF8	00000F20			957+	DC A(IN10)	address of instruction
00000EFC	00000F26			958+	DC A(IN10+6)	address of v2 source
00000F00	00000F36			959+	DC A(IN10+22)	address of v3 source
00000F04	00000F46			960+	DC A(IN10+38)	address of v4
				961+*		
00000F08				962+X10	DS 0F	
00000F08	7FE5C9E2 E3D94040			963+CMT10	DC CL24' "VISTR V1, V2, 0"'	
00000F10	E5F16BE5 F26BF07F					
00000F18	40404040 40404040					
00000F20				964+IN10	DC 0F	zvector instruction for performance test
00000F20				965+	DROP R5	
00000F20	E712 0000 005C			966	VISTR V1, V2, 0	
00000F26	AAAAAAAA AAAAAAAAAA			967	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
00000F2E	AAAAAAAA AAAAAAAAAA					
00000F36	AABBBBAA AABBAAAA			968	DC XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA'	v3
00000F3E	BBAAAABB AAAABBA					
00000F46	00000000 00000002			969	DC XL16' 0000000000000002 0000000000000000'	v4
00000F4E	00000000 00000000					
				970		
				971 *	-----	
				972 *	E75F VSEG - Vector Sign Extend To Doubleword	
				973 *	-----	
				974		
				975	PTEST ' "VSEG V1, V2, 0"'	
00000F58				976+	DS OFD	
00000F58		00000F58		977+	USING *, R5	base for test data and test routine
00000F58	00000F78			978+T11	DC A(X11)	address of test routine
00000F5C	000B			979+	DC H' 11'	test number
00000F5E	0000			980+	DC H' 00'	
00000F60	0012			981+	DC H' 18'	length of comment
00000F64	00000F78			982+	DC A(CMT11)	address of comment
00000F68	00000F90			983+	DC A(IN11)	address of instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00000F6C	00000F96			984+	DC	A(IN11+6)	address of v2 source
00000F70	00000FA6			985+	DC	A(IN11+22)	address of v3 source
00000F74	00000FB6			986+	DC	A(IN11+38)	address of v4
				987+*			
00000F78				988+X11	DS	0F	
00000F78	7FE5E2C5 C7404040			989+CMF11	DC	CL24' "VSEG V1, V2, 0"'	
00000F80	E5F16BE5 F26BF07F						
00000F88	40404040 40404040						
00000F90				990+IN11	DC	0F	zvector instruction for performance test
00000F90				991+	DROP	R5	
00000F90	E712 0000 005F			992	VSEG	V1, V2, 0	
00000F96	AAAAAAAA AAAAAAAAAA			993	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
00000F9E	AAAAAAAA AAAAAAAAAA						
00000FA6	AABBBBAA AABBBAAA			994	DC	XL16' AABBBBAAAABBBAAA BBAAAABBBAAAABBBAA'	v3
00000FAE	BBAAAABB AAAABBBAA						
00000FB6	00000000 00000002			995	DC	XL16' 0000000000000002 0000000000000000'	v4
00000FBE	00000000 00000000						
				996			
				997 *			
				998 *	E760 VMRL	- Vector Merge Low	
				999 *			
				1000			
				1001	PTEST	' "VMRL V1, V2, V3, 0"'	
00000FC8				1002+	DS	0FD	
00000FC8		00000FC8		1003+	USING	*, R5	base for test data and test routine
00000FC8	00000FE8			1004+T12	DC	A(X12)	address of test routine
00000FCC	000C			1005+	DC	H' 12'	test number
00000FCE	0000			1006+	DC	H' 00'	
00000FD0	0015			1007+	DC	H' 21'	length of comment
00000FD4	00000FE8			1008+	DC	A(CMF12)	address of comment
00000FD8	00001000			1009+	DC	A(IN12)	address of instruction
00000FDC	00001006			1010+	DC	A(IN12+6)	address of v2 source
00000FE0	00001016			1011+	DC	A(IN12+22)	address of v3 source
00000FE4	00001026			1012+	DC	A(IN12+38)	address of v4
				1013+*			
00000FE8				1014+X12	DS	0F	
00000FE8	7FE5D4D9 D3404040			1015+CMF12	DC	CL24' "VMRL V1, V2, V3, 0"'	
00000FF0	E5F16BE5 F26BE5F3						
00000FF8	6BF07F40 40404040						
00001000				1016+IN12	DC	0F	zvector instruction for performance test
00001000				1017+	DROP	R5	
00001000	E712 3000 0060			1018	VMRL	V1, V2, V3, 0	
00001006	AAAAAAAA AAAAAAAAAA			1019	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
0000100E	AAAAAAAA AAAAAAAAAA						
00001016	AABBBBAA AABBBAAA			1020	DC	XL16' AABBBBAAAABBBAAA BBAAAABBBAAAABBBAA'	v3
0000101E	BBAAAABB AAAABBBAA						
00001026	00000000 00000002			1021	DC	XL16' 0000000000000002 0000000000000000'	v4
0000102E	00000000 00000000						
				1022			
				1023 *			
				1024 *	E761 VMRH	- Vector Merge High	
				1025 *			
				1026			
				1027	PTEST	' "VMRH V1, V2, V3, 0"'	
00001038				1028+	DS	0FD	
00001038		00001038		1029+	USING	*, R5	base for test data and test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001038	00001058			1030+T13	DC	A(X13) address of test routine
0000103C	000D			1031+	DC	H' 13' test number
0000103E	0000			1032+	DC	H' 00'
00001040	0015			1033+	DC	H' 21' length of comment
00001044	00001058			1034+	DC	A(CMT13) address of comment
00001048	00001070			1035+	DC	A(IN13) address of instruction
0000104C	00001076			1036+	DC	A(IN13+6) address of v2 source
00001050	00001086			1037+	DC	A(IN13+22) address of v3 source
00001054	00001096			1038+	DC	A(IN13+38) address of v4
				1039+*		
00001058				1040+X13	DS	0F
00001058	7FE5D4D9 C8404040			1041+CMT13	DC	CL24' "VMRH V1, V2, V3, 0"
00001060	E5F16BE5 F26BE5F3					
00001068	6BF07F40 40404040					
00001070				1042+IN13	DC	0F zvector instruction for performance test
00001070				1043+	DROP	R5
00001070	E712 3000 0061			1044	VMRH	V1, V2, V3, 0
00001076	AAAAAAAA AAAAAAAAAA			1045	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA' v2
0000107E	AAAAAAAA AAAAAAAAAA					
00001086	AABBBBAA AABBAAAA			1046	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA' v3
0000108E	BBAAAABB AAAABBA					
00001096	00000000 00000002			1047	DC	XL16' 0000000000000002 0000000000000000' v4
0000109E	00000000 00000000					
				1048		
				1049 *		-----
				1050 *		E764 VSUM - Vector Sum Across Word
				1051 *		-----
				1052		
				1053	PTEST	' "VSUM V1, V2, V3, 0"
000010A8				1054+	DS	0FD
000010A8		000010A8		1055+	USING	*, R5
000010A8	000010C8			1056+T14	DC	A(X14) base for test data and test routine
000010AC	000E			1057+	DC	H' 14' address of test routine
000010AE	0000			1058+	DC	H' 00' test number
000010B0	0015			1059+	DC	H' 21' length of comment
000010B4	000010C8			1060+	DC	A(CMT14) address of comment
000010B8	000010E0			1061+	DC	A(IN14) address of instruction
000010BC	000010E6			1062+	DC	A(IN14+6) address of v2 source
000010C0	000010F6			1063+	DC	A(IN14+22) address of v3 source
000010C4	00001106			1064+	DC	A(IN14+38) address of v4
				1065+*		
000010C8				1066+X14	DS	0F
000010C8	7FE5E2E4 D4404040			1067+CMT14	DC	CL24' "VSUM V1, V2, V3, 0"
000010D0	E5F16BE5 F26BE5F3					
000010D8	6BF07F40 40404040					
000010E0				1068+IN14	DC	0F zvector instruction for performance test
000010E0				1069+	DROP	R5
000010E0	E712 3000 0064			1070	VSUM	V1, V2, V3, 0
000010E6	AAAAAAAA AAAAAAAAAA			1071	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA' v2
000010EE	AAAAAAAA AAAAAAAAAA					
000010F6	AABBBBAA AABBAAAA			1072	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA' v3
000010FE	BBAAAABB AAAABBA					
00001106	00000000 00000002			1073	DC	XL16' 0000000000000002 0000000000000000' v4
0000110E	00000000 00000000					
				1074		
				1075 *		-----

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
1076 * E765 VSUMG - Vector Sum Across Doubleword					
1077 *-----					
1078					
00001118				1079 PTEST ' "VSUMG V1, V2, V3, 1"'	
00001118		00001118		1080+ DS OFD	
00001118	00001138			1081+ USING *, R5	base for test data and test routine
0000111C	000F			1082+T15 DC A(X15)	address of test routine
0000111E	0000			1083+ DC H' 15'	test number
00001120	0015			1084+ DC H' 00'	
00001124	00001138			1085+ DC H' 21'	length of comment
00001128	00001150			1086+ DC A(CMF15)	address of comment
0000112C	00001156			1087+ DC A(IN15)	address of instruction
00001130	00001166			1088+ DC A(IN15+6)	address of v2 source
00001134	00001176			1089+ DC A(IN15+22)	address of v3 source
				1090+ DC A(IN15+38)	address of v4
				1091+*	
00001138				1092+X15 DS OF	
00001138	7FE5E2E4 D4C74040			1093+CMF15 DC CL24' "VSUMG V1, V2, V3, 1"'	
00001140	E5F16BE5 F26BE5F3				
00001148	6BF17F40 40404040				
00001150				1094+IN15 DC OF	zvector instruction for performance test
00001150				1095+ DROP R5	
00001150	E712 3000 1065			1096 VSUMG V1, V2, V3, 1	
00001156	AAAAAAAA AAAAAAAAAA			1097 DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
0000115E	AAAAAAAA AAAAAAAAAA				
00001166	AABBBBAA AABBBAAA			1098 DC XL16' AABBBBAAAABBBAAA BBAAAABBBAAAABBBAA'	v3
0000116E	BBAAAABB AAAABBBAA				
00001176	00000000 00000002			1099 DC XL16' 00000000000000002 0000000000000000'	v4
0000117E	00000000 00000000				
1100					
1101 *-----					
1102 * E770 VESLV - Vector Element Shift Left Vector					
1103 *-----					
1104					
				1105 PTEST ' "VESLV V1, V2, V3, 0"'	
00001188				1106+ DS OFD	
00001188		00001188		1107+ USING *, R5	base for test data and test routine
00001188	000011A8			1108+T16 DC A(X16)	address of test routine
0000118C	0010			1109+ DC H' 16'	test number
0000118E	0000			1110+ DC H' 00'	
00001190	0015			1111+ DC H' 21'	length of comment
00001194	000011A8			1112+ DC A(CMF16)	address of comment
00001198	000011C0			1113+ DC A(IN16)	address of instruction
0000119C	000011C6			1114+ DC A(IN16+6)	address of v2 source
000011A0	000011D6			1115+ DC A(IN16+22)	address of v3 source
000011A4	000011E6			1116+ DC A(IN16+38)	address of v4
				1117+*	
000011A8				1118+X16 DS OF	
000011A8	7FE5C5E2 D3E54040			1119+CMF16 DC CL24' "VESLV V1, V2, V3, 0"'	
000011B0	E5F16BE5 F26BE5F3				
000011B8	6BF07F40 40404040				
000011C0				1120+IN16 DC OF	zvector instruction for performance test
000011C0				1121+ DROP R5	
000011C0	E712 3000 0070			1122 VESLV V1, V2, V3, 0	
000011C6	01010101 01010101			1123 DC XL16' 0101010101010101 0101010101010101'	v2
000011CE	01010101 01010101				

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000011D6	00010203 04050607			1124	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3	
000011DE	08090A0B 0C0D0E0F							
000011E6	00000000 00000002			1125	DC	XL16' 00000000000000002 0000000000000000'	v4	
000011EE	00000000 00000000							
				1126				
				1127 *				
				1128 *	E772 VERIM - Vector Element Rotate and Insert Under Mask			
				1129 *				
				1130				
000011F8				1131	PTEST	' "VERIM V1, V2, V3, V4, 0"'		
000011F8		000011F8		1132+	DS	0FD		
000011F8	00001218			1133+	USING	*, R5	base for test data and test routine	
000011FC	0011			1134+T17	DC	A(X17)	address of test routine	
000011FE	0000			1135+	DC	H' 17'	test number	
00001200	0018			1136+	DC	H' 00'		
00001204	00001218			1137+	DC	H' 24'	length of comment	
00001208	00001230			1138+	DC	A(CMF17)	address of comment	
0000120C	00001236			1139+	DC	A(IN17)	address of instruction	
00001210	00001246			1140+	DC	A(IN17+6)	address of v2 source	
00001214	00001256			1141+	DC	A(IN17+22)	address of v3 source	
				1142+	DC	A(IN17+38)	address of v4	
				1143+*				
00001218				1144+X17	DS	0F		
00001218	7FE5C5D9 C9D44040			1145+CMF17	DC	CL24' "VERIM V1, V2, V3, V4, 0"'		
00001220	E5F16BE5 F26BE5F3							
00001228	6BE5F46B F07F4040							
00001230				1146+IN17	DC	0F	zvector instruction for performance test	
00001230				1147+	DROP	R5		
00001230	E712 3004 0072			1148	VERIM	V1, V2, V3, V4, 0		
00001236	01010101 01010101			1149	DC	XL16' 0101010101010101 0101010101010101'	v2	
0000123E	01010101 01010101							
00001246	00010203 04050607			1150	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v3	
0000124E	08090A0B 0C0D0E0F							
00001256	00000000 00000002			1151	DC	XL16' 00000000000000002 0000000000000000'	v4	
0000125E	00000000 00000000							
				1152				
				1153 *				
				1154 *	E775 VSLB - Vector Shift Left By Byte			
				1155 *				
				1156				
00001268				1157	PTEST	' "VSLB V1, V2, V3"'		
00001268		00001268		1158+	DS	0FD		
00001268	00001288			1159+	USING	*, R5	base for test data and test routine	
0000126C	0012			1160+T18	DC	A(X18)	address of test routine	
0000126E	0000			1161+	DC	H' 18'	test number	
00001270	0013			1162+	DC	H' 00'		
00001274	00001288			1163+	DC	H' 19'	length of comment	
00001278	000012A0			1164+	DC	A(CMF18)	address of comment	
0000127C	000012A6			1165+	DC	A(IN18)	address of instruction	
00001280	000012B6			1166+	DC	A(IN18+6)	address of v2 source	
00001284	000012C6			1167+	DC	A(IN18+22)	address of v3 source	
				1168+	DC	A(IN18+38)	address of v4	
				1169+*				
00001288				1170+X18	DS	0F		
00001288	7FE5E2D3 C2404040			1171+CMF18	DC	CL24' "VSLB V1, V2, V3"'		
00001290	E5F16BE5 F26BE5F3							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
00001298	7F404040 40404040				
000012A0				1172+IN18	DC 0F zvector instruction for performance test
000012A0				1173+	DROP R5
000012A0	E712 3000 0075			1174	VSLB V1, V2, V3
000012A6	AAAAAAAA AAAAAAAAAA			1175	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA' v2
000012AE	AAAAAAAA AAAAAAAAAA				
000012B6	00000000 00000002			1176	DC XL16' 0000000000000002 0000000000000000' v3
000012BE	00000000 00000000				
000012C6	00000000 00000002			1177	DC XL16' 0000000000000002 0000000000000000' v4
000012CE	00000000 00000000				
				1178	
				1179 *	-----
				1180 *	E777 VSLDB - Vector Shift Left Double By Byte
				1181 *	-----
				1182	
				1183	PTEST ' "VSLDB V1, V2, V3, 5"'
000012D8				1184+	DS OFD
000012D8		000012D8		1185+	USING *, R5 base for test data and test routine
000012D8	000012F8			1186+T19	DC A(X19) address of test routine
000012DC	0013			1187+	DC H' 19' test number
000012DE	0000			1188+	DC H' 00'
000012E0	0015			1189+	DC H' 21' length of comment
000012E4	000012F8			1190+	DC A(CMF19) address of comment
000012E8	00001310			1191+	DC A(IN19) address of instruction
000012EC	00001316			1192+	DC A(IN19+6) address of v2 source
000012F0	00001326			1193+	DC A(IN19+22) address of v3 source
000012F4	00001336			1194+	DC A(IN19+38) address of v4
				1195+*	
000012F8				1196+X19	DS 0F
000012F8	7FE5E2D3 C4C24040			1197+CMF19	DC CL24' "VSLDB V1, V2, V3, 5"'
00001300	E5F16BE5 F26BE5F3				
00001308	6BF57F40 40404040				
00001310				1198+IN19	DC 0F zvector instruction for performance test
00001310				1199+	DROP R5
00001310	E712 3005 0077			1200	VSLB V1, V2, V3, 5
00001316	AAAAAAAA AAAAAAAAAA			1201	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA' v2
0000131E	AAAAAAAA AAAAAAAAAA				
00001326	00000000 00000002			1202	DC XL16' 0000000000000002 0000000000000000' v3
0000132E	00000000 00000000				
00001336	00000000 00000002			1203	DC XL16' 0000000000000002 0000000000000000' v4
0000133E	00000000 00000000				
				1204	
				1205 *	-----
				1206 *	E77D VSRLB - Vector Shift Right Logical By Byte
				1207 *	-----
				1208	
				1209	PTEST ' "VSRLB V1, V2, V3"'
00001348				1210+	DS OFD
00001348		00001348		1211+	USING *, R5 base for test data and test routine
00001348	00001368			1212+T20	DC A(X20) address of test routine
0000134C	0014			1213+	DC H' 20' test number
0000134E	0000			1214+	DC H' 00'
00001350	0013			1215+	DC H' 19' length of comment
00001354	00001368			1216+	DC A(CMF20) address of comment
00001358	00001380			1217+	DC A(IN20) address of instruction
0000135C	00001386			1218+	DC A(IN20+6) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001360	00001396			1219+	DC	A(IN20+22)	address of v3 source
00001364	000013A6			1220+	DC	A(IN20+38)	address of v4
				1221+*			
00001368				1222+X20	DS	0F	
00001368	7FE5E2D9 D3C24040			1223+CMF20	DC	CL24' "VSRLB V1, V2, V3"	
00001370	E5F16BE5 F26BE5F3						
00001378	7F404040 40404040						
00001380				1224+IN20	DC	0F	zvector instruction for performance test
00001380				1225+	DROP	R5	
00001380	E712 3000 007D			1226	VSRLB	V1, V2, V3	
00001386	AAAAAAAA AAAAAAAAAA			1227	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
0000138E	AAAAAAAA AAAAAAAAAA						
00001396	00000000 00000002			1228	DC	XL16' 0000000000000002 0000000000000000'	v3
0000139E	00000000 00000000						
000013A6	00000000 00000002			1229	DC	XL16' 0000000000000002 0000000000000000'	v4
000013AE	00000000 00000000						
				1230			
				1231 *			
				1232 *	E77F VSRAB	- Vector Shift Right Arithmetic By Byte	
				1233 *			
				1234			
				1235	PTEST	' "VSRAB V1, V2, V3"'	
000013B8				1236+	DS	0FD	
000013B8		000013B8		1237+	USING	*, R5	base for test data and test routine
000013B8	000013D8			1238+T21	DC	A(X21)	address of test routine
000013BC	0015			1239+	DC	H' 21'	test number
000013BE	0000			1240+	DC	H' 00'	
000013C0	0013			1241+	DC	H' 19'	length of comment
000013C4	000013D8			1242+	DC	A(CMF21)	address of comment
000013C8	000013F0			1243+	DC	A(IN21)	address of instruction
000013CC	000013F6			1244+	DC	A(IN21+6)	address of v2 source
000013D0	00001406			1245+	DC	A(IN21+22)	address of v3 source
000013D4	00001416			1246+	DC	A(IN21+38)	address of v4
				1247+*			
000013D8				1248+X21	DS	0F	
000013D8	7FE5E2D9 C1C24040			1249+CMF21	DC	CL24' "VSRAB V1, V2, V3"	
000013E0	E5F16BE5 F26BE5F3						
000013E8	7F404040 40404040						
000013F0				1250+IN21	DC	0F	zvector instruction for performance test
000013F0				1251+	DROP	R5	
000013F0	E712 3000 007F			1252	VSRAB	V1, V2, V3	
000013F6	AAAAAAAA AAAAAAAAAA			1253	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
000013FE	AAAAAAAA AAAAAAAAAA						
00001406	00000000 00000002			1254	DC	XL16' 0000000000000002 0000000000000000'	v3
0000140E	00000000 00000000						
00001416	00000000 00000002			1255	DC	XL16' 0000000000000002 0000000000000000'	v4
0000141E	00000000 00000000						
				1256			
				1257 *			
				1258 *	E780 VFEE	- Vector Find Element Equal	
				1259 *			
				1260			
				1261	PTEST	' "VFEE V1, V2, V3, 0"'	
00001428				1262+	DS	0FD	
00001428		00001428		1263+	USING	*, R5	base for test data and test routine
00001428	00001448			1264+T22	DC	A(X22)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000142C	0016			1265+	DC	H' 22'	test number
0000142E	0000			1266+	DC	H' 00'	
00001430	0015			1267+	DC	H' 21'	length of comment
00001434	00001448			1268+	DC	A(CMF22)	address of comment
00001438	00001460			1269+	DC	A(IN22)	address of instruction
0000143C	00001466			1270+	DC	A(IN22+6)	address of v2 source
00001440	00001476			1271+	DC	A(IN22+22)	address of v3 source
00001444	00001486			1272+	DC	A(IN22+38)	address of v4
				1273+*			
00001448				1274+X22	DS	0F	
00001448	7FE5C6C5 C5404040			1275+CMF22	DC	CL24' "VFEE V1, V2, V3, 0"	
00001450	E5F16BE5 F26BE5F3						
00001458	6BF07F40 40404040						
00001460				1276+IN22	DC	0F	zvector instruction for performance test
00001460				1277+	DROP	R5	
00001460	E712 3000 0080			1278	VFEE	V1, V2, V3, 0	
00001466	AAAAAAAA AAAAAAAAAA			1279	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
0000146E	AAAAAAAA AAAAAAAAAA						
00001476	00000000 00000002			1280	DC	XL16' 0000000000000002 00000000000000AA'	v3
0000147E	00000000 000000AA						
00001486	00000000 00000002			1281	DC	XL16' 0000000000000002 0000000000000000'	v4
0000148E	00000000 00000000						
				1282			
				1283 *			
				1284 *	E781 VFENE	- Vector Find Element Not Equal	
				1285 *			
				1286			
				1287	PTEST	' "VFENE V1, V2, V3, 0"	
00001498				1288+	DS	0FD	
00001498		00001498		1289+	USING	*, R5	base for test data and test routine
00001498	000014B8			1290+T23	DC	A(X23)	address of test routine
0000149C	0017			1291+	DC	H' 23'	test number
0000149E	0000			1292+	DC	H' 00'	
000014A0	0015			1293+	DC	H' 21'	length of comment
000014A4	000014B8			1294+	DC	A(CMF23)	address of comment
000014A8	000014D0			1295+	DC	A(IN23)	address of instruction
000014AC	000014D6			1296+	DC	A(IN23+6)	address of v2 source
000014B0	000014E6			1297+	DC	A(IN23+22)	address of v3 source
000014B4	000014F6			1298+	DC	A(IN23+38)	address of v4
				1299+*			
000014B8				1300+X23	DS	0F	
000014B8	7FE5C6C5 D5C54040			1301+CMF23	DC	CL24' "VFENE V1, V2, V3, 0"	
000014C0	E5F16BE5 F26BE5F3						
000014C8	6BF07F40 40404040						
000014D0				1302+IN23	DC	0F	zvector instruction for performance test
000014D0				1303+	DROP	R5	
000014D0	E712 3000 0081			1304	VFENE	V1, V2, V3, 0	
000014D6	AAAAAAAA AAAAAAAAAA			1305	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
000014DE	AAAAAAAA AAAAAAAAAA						
000014E6	AAAAAAAA AAAAAAAAAA			1306	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAABB'	v3
000014EE	AAAAAAAA AAAAAABB						
000014F6	00000000 00000002			1307	DC	XL16' 0000000000000002 0000000000000000'	v4
000014FE	00000000 00000000						
				1308			
				1309 *			
				1310 *	E782 VFAE	- Vector Find Any Element Equal	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1311 *	-----
				1312	
00001508				1313	PTEST ' "VFAE V1, V2, V3, 0"'
00001508		00001508		1314+	DS OFD
00001508	00001528			1315+	USING *, R5
0000150C	0018			1316+T24	DC A(X24)
0000150E	0000			1317+	DC H' 24'
00001510	0015			1318+	DC H' 00'
00001514	00001528			1319+	DC H' 21'
00001518	00001540			1320+	DC A(CMT24)
0000151C	00001546			1321+	DC A(IN24)
00001520	00001556			1322+	DC A(IN24+6)
00001524	00001566			1323+	DC A(IN24+22)
				1324+	DC A(IN24+38)
				1325+*	
00001528				1326+X24	DS OF
00001528	7FE5C6C1 C5404040			1327+CMF24	DC CL24' "VFAE V1, V2, V3, 0"'
00001530	E5F16BE5 F26BE5F3				
00001538	6BF07F40 40404040				
00001540				1328+IN24	DC OF
00001540				1329+	DROP R5
00001540	E712 3000 0082			1330	VFAE V1, V2, V3, 0
00001546	AAAAAAAA AAAAAAAAAA			1331	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAABB' v2
0000154E	AAAAAAAA AAAAAABB				
00001556	00000000 00000002			1332	DC XL16' 0000000000000002 00000000000000BB' v3
0000155E	00000000 000000BB				
00001566	00000000 00000002			1333	DC XL16' 0000000000000002 0000000000000000' v4
0000156E	00000000 00000000				
				1334	
				1335 *	-----
				1336 *	E785 VBPERM - Vector Bit Permute
				1337 *	-----
				1338	
00001578				1339	PTEST ' "VBPERM V1, V2, V3"'
00001578		00001578		1340+	DS OFD
00001578	00001598			1341+	USING *, R5
0000157C	0019			1342+T25	DC A(X25)
0000157E	0000			1343+	DC H' 25'
00001580	0013			1344+	DC H' 00'
00001584	00001598			1345+	DC H' 19'
00001588	000015B0			1346+	DC A(CMF25)
0000158C	000015B6			1347+	DC A(IN25)
00001590	000015C6			1348+	DC A(IN25+6)
00001594	000015D6			1349+	DC A(IN25+22)
				1350+	DC A(IN25+38)
				1351+*	
00001598				1352+X25	DS OF
00001598	7FE5C2D7 C5D9D440			1353+CMF25	DC CL24' "VBPERM V1, V2, V3"'
000015A0	E5F16BE5 F26BE5F3				
000015A8	7F404040 40404040				
000015B0				1354+IN25	DC OF
000015B0				1355+	DROP R5
000015B0	E712 3000 0085			1356	VBPERM V1, V2, V3
000015B6	AAAAAAAA AAAAAAAAAA			1357	DC XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAA' v2
000015BE	AAAAAAAA AAAAAAAAAA				
000015C6	00000000 00000002			1358	DC XL16' 0000000000000002 0000000000000000' v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000015CE	00000000	00000000						
000015D6	00000000	00000002		1359	DC	XL16'	00000000000000002	0000000000000000' v4
000015DE	00000000	00000000						
				1360				
				1361	*	-----		
				1362	*	VSTRS - Vector String Search		
				1363	*	-----		
				1364				
000015E8				1365	PTEST	' "VSTRS V1, V2, V3, V4, 0, 2"'		
000015E8		000015E8		1366+	DS	0FD		
000015E8	00001608			1367+	USING	*, R5		base for test data and test routine
000015EC	001A			1368+T26	DC	A(X26)		address of test routine
000015EE	0000			1369+	DC	H' 26'		test number
000015F0	001A			1370+	DC	H' 00'		
000015F4	00001608			1371+	DC	H' 26'		length of comment
000015F8	00001620			1372+	DC	A(CMT26)		address of comment
000015FC	00001626			1373+	DC	A(IN26)		address of instruction
00001600	00001636			1374+	DC	A(IN26+6)		address of v2 source
00001604	00001646			1375+	DC	A(IN26+22)		address of v3 source
				1376+	DC	A(IN26+38)		address of v4
				1377+*				
00001608				1378+X26	DS	0F		
00001608	7FE5E2E3	D9E24040		1379+CMT26	DC	CL24' "VSTRS V1, V2, V3, V4, 0, 2"'		
00001610	E5F16BE5	F26BE5F3						
00001618	6BE5F46B	F06BF27F						
00001620				1380+IN26	DC	0F		zvector instruction for performance test
00001620				1381+	DROP	R5		
00001620	E712 3020 408B			1382	VSTRS	V1, V2, V3, V4, 0, 2		
00001626	AAAAAAAA	AAAAAAAA		1383	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'		v2
0000162E	AAAAAAAA	AAAAAAAA						
00001636	AABBBBAA	AABBAAAA		1384	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAAAABBAA'		v3
0000163E	BBAAAABB	AAAABBAA						
00001646	00000000	00000002		1385	DC	XL16' 00000000000000002 0000000000000000'		v4
0000164E	00000000	00000000						
				1386				
				1387	*	-----		
				1388	*	E78C VPERM - Vector Permute		
				1389	*	-----		
				1390				
00001658				1391	PTEST	' "VPERM V1, V2, V3, V4"'		
00001658		00001658		1392+	DS	0FD		
00001658	00001678			1393+	USING	*, R5		base for test data and test routine
0000165C	001B			1394+T27	DC	A(X27)		address of test routine
0000165E	0000			1395+	DC	H' 27'		test number
00001660	0016			1396+	DC	H' 00'		
00001664	00001678			1397+	DC	H' 22'		length of comment
00001668	00001690			1398+	DC	A(CMT27)		address of comment
0000166C	00001696			1399+	DC	A(IN27)		address of instruction
00001670	000016A6			1400+	DC	A(IN27+6)		address of v2 source
00001674	000016B6			1401+	DC	A(IN27+22)		address of v3 source
				1402+	DC	A(IN27+38)		address of v4
				1403+*				
00001678				1404+X27	DS	0F		
00001678	7FE5D7C5	D9D44040		1405+CMT27	DC	CL24' "VPERM V1, V2, V3, V4"'		
00001680	E5F16BE5	F26BE5F3						
00001688	6BE5F47F	40404040						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001690				1406+IN27	DC	0F	zvector instruction for performance test
00001690				1407+	DROP	R5	
00001690	E712 3000 408C			1408	VPERM	V1, V2, V3, v4	
00001696	AAAAAAAA AAAAAAAAAA			1409	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
0000169E	AAAAAAAA AAAAAAAAAA						
000016A6	AABBBBAA AABBAAAA			1410	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA'	v3
000016AE	BBAAAABB AAAABBA						
000016B6	00000000 00000002			1411	DC	XL16' 0000000000000002 0000000000000000'	v4
000016BE	00000000 00000000						
				1412			
				1413 *			
				1414 *	E794 VPK	- Vector Pack	
				1415 *			
				1416			
				1417	PTEST	' "VPK V1, V2, V3, 1"'	
000016C8				1418+	DS	0FD	
000016C8		000016C8		1419+	USING	*, R5	base for test data and test routine
000016C8	000016E8			1420+T28	DC	A(X28)	address of test routine
000016CC	001C			1421+	DC	H' 28'	test number
000016CE	0000			1422+	DC	H' 00'	
000016D0	0015			1423+	DC	H' 21'	length of comment
000016D4	000016E8			1424+	DC	A(CMF28)	address of comment
000016D8	00001700			1425+	DC	A(IN28)	address of instruction
000016DC	00001706			1426+	DC	A(IN28+6)	address of v2 source
000016E0	00001716			1427+	DC	A(IN28+22)	address of v3 source
000016E4	00001726			1428+	DC	A(IN28+38)	address of v4
				1429+*			
000016E8				1430+X28	DS	0F	
000016E8	7FE5D7D2 40404040			1431+CMF28	DC	CL24' "VPK V1, V2, V3, 1"'	
000016F0	E5F16BE5 F26BE5F3						
000016F8	6BF17F40 40404040						
00001700				1432+IN28	DC	0F	zvector instruction for performance test
00001700				1433+	DROP	R5	
00001700	E712 3000 1094			1434	VPK	V1, V2, V3, 1	
00001706	AAAAAAAA AAAAAAAAAA			1435	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
0000170E	AAAAAAAA AAAAAAAAAA						
00001716	AABBBBAA AABBAAAA			1436	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA'	v3
0000171E	BBAAAABB AAAABBA						
00001726	00000000 00000002			1437	DC	XL16' 0000000000000002 0000000000000000'	v4
0000172E	00000000 00000000						
				1438			
				1439 *			
				1440 *	E795 VPKLS	- Vector Pack Logical Saturate	
				1441 *			
				1442			
				1443	PTEST	' "VPKLS V1, V2, V3, 1, 2"'	
00001738				1444+	DS	0FD	
00001738		00001738		1445+	USING	*, R5	base for test data and test routine
00001738	00001758			1446+T29	DC	A(X29)	address of test routine
0000173C	001D			1447+	DC	H' 29'	test number
0000173E	0000			1448+	DC	H' 00'	
00001740	0017			1449+	DC	H' 23'	length of comment
00001744	00001758			1450+	DC	A(CMF29)	address of comment
00001748	00001770			1451+	DC	A(IN29)	address of instruction
0000174C	00001776			1452+	DC	A(IN29+6)	address of v2 source
00001750	00001786			1453+	DC	A(IN29+22)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001754	00001796			1454+	DC	A(IN29+38)	address of v4
				1455+*			
00001758				1456+X29	DS	0F	
00001758	7FE5D7D2 D3E24040			1457+CMF29	DC	CL24' "VPKLS V1, V2, V3, 1, 2"'	
00001760	E5F16BE5 F26BE5F3						
00001768	6BF16BF2 7F404040						
00001770				1458+IN29	DC	0F	zvector instruction for performance test
00001770				1459+	DROP	R5	
00001770	E712 3020 1095			1460	VPKLS	V1, V2, V3, 1, 2	
00001776	AAAAAAAA AAAAAAAAAA			1461	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
0000177E	AAAAAAAA AAAAAAAAAA						
00001786	AABBBBAA AABBAAAA			1462	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA'	v3
0000178E	BBAAAABB AAAABBA						
00001796	00000000 00000002			1463	DC	XL16' 00000000000000002 0000000000000000'	v4
0000179E	00000000 00000000						
				1464			
				1465 *			
				1466 *	E797 VPKS	- Vector Pack Saturate	
				1467 *			
				1468			
				1469	PTEST	' "VPKS V1, V2, V3, 1, 2"'	
000017A8				1470+	DS	0FD	
000017A8		000017A8		1471+	USING	*, R5	base for test data and test routine
000017A8	000017C8			1472+T30	DC	A(X30)	address of test routine
000017AC	001E			1473+	DC	H' 30'	test number
000017AE	0000			1474+	DC	H' 00'	
000017B0	0017			1475+	DC	H' 23'	length of comment
000017B4	000017C8			1476+	DC	A(CMF30)	address of comment
000017B8	000017E0			1477+	DC	A(IN30)	address of instruction
000017BC	000017E6			1478+	DC	A(IN30+6)	address of v2 source
000017C0	000017F6			1479+	DC	A(IN30+22)	address of v3 source
000017C4	00001806			1480+	DC	A(IN30+38)	address of v4
				1481+*			
000017C8				1482+X30	DS	0F	
000017C8	7FE5D7D2 E2404040			1483+CMF30	DC	CL24' "VPKS V1, V2, V3, 1, 2"'	
000017D0	E5F16BE5 F26BE5F3						
000017D8	6BF16BF2 7F404040						
000017E0				1484+IN30	DC	0F	zvector instruction for performance test
000017E0				1485+	DROP	R5	
000017E0	E712 3020 1097			1486	VPKS	V1, V2, V3, 1, 2	
000017E6	AAAAAAAA AAAAAAAAAA			1487	DC	XL16' AAAAAAAAAAAAAAAAAA AAAAAAAAAAAAAAAAAA'	v2
000017EE	AAAAAAAA AAAAAAAAAA						
000017F6	AABBBBAA AABBAAAA			1488	DC	XL16' AABBBBAAAABBAAAA BBAAAABBAABBAABBA'	v3
000017FE	BBAAAABB AAAABBA						
00001806	00000000 00000002			1489	DC	XL16' 00000000000000002 0000000000000000'	v4
0000180E	00000000 00000000						
				1490			
				1491 *			
				1492 *	E7A1 VMLH	- Vector Multiply Logical High	
				1493 *			
				1494			
				1495	PTEST	' "VMLH V1, V2, V3, 0"'	
00001818				1496+	DS	0FD	
00001818		00001818		1497+	USING	*, R5	base for test data and test routine
00001818	00001838			1498+T31	DC	A(X31)	address of test routine
0000181C	001F			1499+	DC	H' 31'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000181E	0000			1500+	DC	H' 00'	
00001820	0015			1501+	DC	H' 21'	length of comment
00001824	00001838			1502+	DC	A(CMT31)	address of comment
00001828	00001850			1503+	DC	A(IN31)	address of instruction
0000182C	00001856			1504+	DC	A(IN31+6)	address of v2 source
00001830	00001866			1505+	DC	A(IN31+22)	address of v3 source
00001834	00001876			1506+	DC	A(IN31+38)	address of v4
				1507+*			
00001838				1508+X31	DS	0F	
00001838	7FE5D4D3 C8404040			1509+CMT31	DC	CL24' "VMLH V1, V2, V3, 0"	
00001840	E5F16BE5 F26BE5F3						
00001848	6BF07F40 40404040						
00001850				1510+IN31	DC	0F	zvector instruction for performance test
00001850				1511+	DROP	R5	
00001850	E712 3000 00A1			1512	VMLH	V1, V2, V3, 0	
00001856	FF020304 05060750			1513	DC	XL16' FF02030405060750 090A0B780C0D0EFD'	v2
0000185E	090A0B78 0C0D0EFD						
00001866	FF020304 05060750			1514	DC	XL16' FF02030405060750 090A0B780D0E0FFD'	v3
0000186E	090A0B78 0D0E0FFD						
00001876	00000000 00000002			1515	DC	XL16' 0000000000000002 0000000000000000'	v4
0000187E	00000000 00000000						
				1516			
				1517 *			
				1518 * E7A2 VML		- Vector Multiply Low	
				1519 *			
				1520			
				1521	PTEST	' "VML V1, V2, V3, 0"	
00001888				1522+	DS	0FD	
00001888		00001888		1523+	USING	*, R5	base for test data and test routine
00001888	000018A8			1524+T32	DC	A(X32)	address of test routine
0000188C	0020			1525+	DC	H' 32'	test number
0000188E	0000			1526+	DC	H' 00'	
00001890	0015			1527+	DC	H' 21'	length of comment
00001894	000018A8			1528+	DC	A(CMT32)	address of comment
00001898	000018C0			1529+	DC	A(IN32)	address of instruction
0000189C	000018C6			1530+	DC	A(IN32+6)	address of v2 source
000018A0	000018D6			1531+	DC	A(IN32+22)	address of v3 source
000018A4	000018E6			1532+	DC	A(IN32+38)	address of v4
				1533+*			
000018A8				1534+X32	DS	0F	
000018A8	7FE5D4D3 40404040			1535+CMT32	DC	CL24' "VML V1, V2, V3, 0"	
000018B0	E5F16BE5 F26BE5F3						
000018B8	6BF07F40 40404040						
000018C0				1536+IN32	DC	0F	zvector instruction for performance test
000018C0				1537+	DROP	R5	
000018C0	E712 3000 00A2			1538	VML	V1, V2, V3, 0	
000018C6	FF020304 05060750			1539	DC	XL16' FF02030405060750 090A0B780C0D0EFD'	v2
000018CE	090A0B78 0C0D0EFD						
000018D6	FF020304 05060750			1540	DC	XL16' FF02030405060750 090A0B780D0E0FFD'	v3
000018DE	090A0B78 0D0E0FFD						
000018E6	00000000 00000002			1541	DC	XL16' 0000000000000002 0000000000000000'	v4
000018EE	00000000 00000000						
				1542			
				1543 *			
				1544 * E7A3 VMH		- Vector Multiply High	
				1545 *			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
				1546				
				1547	PTEST	' "VMH	V1, V2, V3, 0"	
000018F8				1548+	DS	0FD		
000018F8		000018F8		1549+	USING	*, R5		base for test data and test routine
000018F8	00001918			1550+T33	DC	A(X33)		address of test routine
000018FC	0021			1551+	DC	H' 33'		test number
000018FE	0000			1552+	DC	H' 00'		
00001900	0015			1553+	DC	H' 21'		length of comment
00001904	00001918			1554+	DC	A(CMT33)		address of comment
00001908	00001930			1555+	DC	A(IN33)		address of instruction
0000190C	00001936			1556+	DC	A(IN33+6)		address of v2 source
00001910	00001946			1557+	DC	A(IN33+22)		address of v3 source
00001914	00001956			1558+	DC	A(IN33+38)		address of v4
				1559+*				
00001918				1560+X33	DS	0F		
00001918	7FE5D4C8 40404040			1561+CMT33	DC	CL24' "VMH	V1, V2, V3, 0"	
00001920	E5F16BE5 F26BE5F3							
00001928	6BF07F40 40404040							
00001930				1562+IN33	DC	0F		zvector instruction for performance test
00001930				1563+	DROP	R5		
00001930	E712 3000 00A3			1564	VMH	V1, V2, V3, 0		
00001936	FF020304 05060750			1565	DC	XL16' FF02030405060750 090A0B780C0D0EFD'		v2
0000193E	090A0B78 0C0D0EFD							
00001946	FF020304 05060750			1566	DC	XL16' FF02030405060750 090A0B780D0E0FFD'		v3
0000194E	090A0B78 0D0E0FFD							
00001956	00000000 00000002			1567	DC	XL16' 00000000000000002 0000000000000000'		v4
0000195E	00000000 00000000							
				1568				
				1569 *				
				1570 * E7A4 VMLE		- Vector Multiply Logical Even		
				1571 *				
				1572				
				1573	PTEST	' "VMLE	V1, V2, V3, 0"	
00001968				1574+	DS	0FD		
00001968		00001968		1575+	USING	*, R5		base for test data and test routine
00001968	00001988			1576+T34	DC	A(X34)		address of test routine
0000196C	0022			1577+	DC	H' 34'		test number
0000196E	0000			1578+	DC	H' 00'		
00001970	0015			1579+	DC	H' 21'		length of comment
00001974	00001988			1580+	DC	A(CMT34)		address of comment
00001978	000019A0			1581+	DC	A(IN34)		address of instruction
0000197C	000019A6			1582+	DC	A(IN34+6)		address of v2 source
00001980	000019B6			1583+	DC	A(IN34+22)		address of v3 source
00001984	000019C6			1584+	DC	A(IN34+38)		address of v4
				1585+*				
00001988				1586+X34	DS	0F		
00001988	7FE5D4D3 C5404040			1587+CMT34	DC	CL24' "VMLE	V1, V2, V3, 0"	
00001990	E5F16BE5 F26BE5F3							
00001998	6BF07F40 40404040							
000019A0				1588+IN34	DC	0F		zvector instruction for performance test
000019A0				1589+	DROP	R5		
000019A0	E712 3000 00A4			1590	VMLE	V1, V2, V3, 0		
000019A6	FF020304 05060750			1591	DC	XL16' FF02030405060750 090A0B780C0D0EFD'		v2
000019AE	090A0B78 0C0D0EFD							
000019B6	FF020304 05060750			1592	DC	XL16' FF02030405060750 090A0B780D0E0FFD'		v3
000019BE	090A0B78 0D0E0FFD							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
000019C6	00000000 00000002			1593	DC	XL16'	000000000000000002 0000000000000000'	v4	
000019CE	00000000 00000000								
				1594					
				1595	*	-----			
				1596	*	E7A5 VML0	- Vector Multiply Logical Odd		
				1597	*	-----			
				1598					
				1599	PTEST	' "VML0	V1, V2, V3, 0"'		
000019D8				1600+	DS	0FD			
000019D8		000019D8		1601+	USING	*, R5		base for test data and test routine	
000019D8	000019F8			1602+T35	DC	A(X35)		address of test routine	
000019DC	0023			1603+	DC	H' 35'		test number	
000019DE	0000			1604+	DC	H' 00'			
000019E0	0015			1605+	DC	H' 21'		length of comment	
000019E4	000019F8			1606+	DC	A(CMT35)		address of comment	
000019E8	00001A10			1607+	DC	A(IN35)		address of instruction	
000019EC	00001A16			1608+	DC	A(IN35+6)		address of v2 source	
000019F0	00001A26			1609+	DC	A(IN35+22)		address of v3 source	
000019F4	00001A36			1610+	DC	A(IN35+38)		address of v4	
				1611+*					
000019F8				1612+X35	DS	0F			
000019F8	7FE5D4D3 D6404040			1613+CMT35	DC	CL24' "VML0	V1, V2, V3, 0"'		
00001A00	E5F16BE5 F26BE5F3								
00001A08	6BF07F40 40404040								
00001A10				1614+IN35	DC	0F		zvector instruction for performance test	
00001A10				1615+	DROP	R5			
00001A10	E712 3000 00A5			1616	VML0	V1, V2, V3, 0			
00001A16	FF020304 05060750			1617	DC	XL16' FF02030405060750 090A0B780C0D0EFD'		v2	
00001A1E	090A0B78 0C0D0EFD								
00001A26	FF020304 05060750			1618	DC	XL16' FF02030405060750 090A0B780D0E0FFD'		v3	
00001A2E	090A0B78 0D0E0FFD								
00001A36	00000000 00000002			1619	DC	XL16' 000000000000000002 0000000000000000'		v4	
00001A3E	00000000 00000000								
				1620					
				1621	*	-----			
				1622	*	E7A6 VME	- Vector Multiply Even		
				1623	*	-----			
				1624					
				1625	PTEST	' "VME	V1, V2, V3, 0"'		
00001A48				1626+	DS	0FD			
00001A48		00001A48		1627+	USING	*, R5		base for test data and test routine	
00001A48	00001A68			1628+T36	DC	A(X36)		address of test routine	
00001A4C	0024			1629+	DC	H' 36'		test number	
00001A4E	0000			1630+	DC	H' 00'			
00001A50	0015			1631+	DC	H' 21'		length of comment	
00001A54	00001A68			1632+	DC	A(CMT36)		address of comment	
00001A58	00001A80			1633+	DC	A(IN36)		address of instruction	
00001A5C	00001A86			1634+	DC	A(IN36+6)		address of v2 source	
00001A60	00001A96			1635+	DC	A(IN36+22)		address of v3 source	
00001A64	00001AA6			1636+	DC	A(IN36+38)		address of v4	
				1637+*					
00001A68				1638+X36	DS	0F			
00001A68	7FE5D4C5 40404040			1639+CMT36	DC	CL24' "VME	V1, V2, V3, 0"'		
00001A70	E5F16BE5 F26BE5F3								
00001A78	6BF07F40 40404040								
00001A80				1640+IN36	DC	0F		zvector instruction for performance test	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001A80				1641+	DROP	R5		
00001A80	E712 3000 00A6			1642	VME	V1, V2, V3, 0		
00001A86	FF020304 05060750			1643	DC	XL16' FF02030405060750 090A0B780C0D0EFD'	v2	
00001A8E	090A0B78 0C0D0EFD							
00001A96	FF020304 05060750			1644	DC	XL16' FF02030405060750 090A0B780D0E0FFD'	v3	
00001A9E	090A0B78 0D0E0FFD							
00001AA6	00000000 00000002			1645	DC	XL16' 00000000000000002 0000000000000000'	v4	
00001AAE	00000000 00000000							
				1646				
				1647 *				
				1648 *	E7A7 VMD	- Vector Multiply Odd		
				1649 *				
				1650				
				1651	PTEST	' "VMD V1, V2, V3, 0"'		
00001AB8				1652+	DS	0FD		
00001AB8		00001AB8		1653+	USING	*, R5	base for test data and test routine	
00001AB8	00001AD8			1654+T37	DC	A(X37)	address of test routine	
00001ABC	0025			1655+	DC	H' 37'	test number	
00001ABE	0000			1656+	DC	H' 00'		
00001AC0	0015			1657+	DC	H' 21'	length of comment	
00001AC4	00001AD8			1658+	DC	A(CMT37)	address of comment	
00001AC8	00001AF0			1659+	DC	A(IN37)	address of instruction	
00001ACC	00001AF6			1660+	DC	A(IN37+6)	address of v2 source	
00001AD0	00001B06			1661+	DC	A(IN37+22)	address of v3 source	
00001AD4	00001B16			1662+	DC	A(IN37+38)	address of v4	
				1663+*				
00001AD8				1664+X37	DS	0F		
00001AD8	7FE5D4D6 40404040			1665+CMT37	DC	CL24' "VMD V1, V2, V3, 0"'		
00001AE0	E5F16BE5 F26BE5F3							
00001AE8	6BF07F40 40404040							
00001AF0				1666+IN37	DC	0F	zvector instruction for performance test	
00001AF0				1667+	DROP	R5		
00001AF0	E712 3000 00A7			1668	VMD	V1, V2, V3, 0		
00001AF6	FF020304 05060750			1669	DC	XL16' FF02030405060750 090A0B780C0D0EFD'	v2	
00001AFE	090A0B78 0C0D0EFD							
00001B06	FF020304 05060750			1670	DC	XL16' FF02030405060750 090A0B780D0E0FFD'	v3	
00001B0E	090A0B78 0D0E0FFD							
00001B16	00000000 00000002			1671	DC	XL16' 00000000000000002 0000000000000000'	v4	
00001B1E	00000000 00000000							
				1672				
				1673 *				
				1674 *	E7A9 VMALH	- Vector Multiply and Add Logical High		
				1675 *				
				1676				
				1677	PTEST	' "VMALH V1, V2, V3, V4, 0"'		
00001B28				1678+	DS	0FD		
00001B28		00001B28		1679+	USING	*, R5	base for test data and test routine	
00001B28	00001B48			1680+T38	DC	A(X38)	address of test routine	
00001B2C	0026			1681+	DC	H' 38'	test number	
00001B2E	0000			1682+	DC	H' 00'		
00001B30	0018			1683+	DC	H' 24'	length of comment	
00001B34	00001B48			1684+	DC	A(CMT38)	address of comment	
00001B38	00001B60			1685+	DC	A(IN38)	address of instruction	
00001B3C	00001B66			1686+	DC	A(IN38+6)	address of v2 source	
00001B40	00001B76			1687+	DC	A(IN38+22)	address of v3 source	
00001B44	00001B86			1688+	DC	A(IN38+38)	address of v4	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1689+*		
00001B48				1690+X38	DS	0F
00001B48	7FE5D4C1 D3C84040			1691+CMF38	DC	CL24' "VMALH V1, V2, V3, V4, 0"
00001B50	E5F16BE5 F26BE5F3					
00001B58	6BE5F46B F07F4040					
00001B60				1692+IN38	DC	0F zvector instruction for performance test
00001B60				1693+	DROP	R5
00001B60	E712 3000 40A9			1694	VMALH	V1, V2, V3, v4, 0
00001B66	FF020304 05060708			1695	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v2
00001B6E	090A0B0C 0D0E0F10					
00001B76	FF020304 05060708			1696	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v3
00001B7E	090A0B0C 0D0E0F10					
00001B86	FF020304 05060708			1697	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v4
00001B8E	090A0B0C 0D0E0F10					
				1698		
				1699 *		
				1700 * E7AA VMAL		- Vector Multiply and Add Low
				1701 *		
				1702		
				1703	PTEST	' "VMAL V1, V2, V3, V4, 0"
00001B98				1704+	DS	0FD
00001B98		00001B98		1705+	USING	*, R5 base for test data and test routine
00001B98	00001BB8			1706+T39	DC	A(X39) address of test routine
00001B9C	0027			1707+	DC	H' 39' test number
00001B9E	0000			1708+	DC	H' 00'
00001BA0	0018			1709+	DC	H' 24' length of comment
00001BA4	00001BB8			1710+	DC	A(CMF39) address of comment
00001BA8	00001BD0			1711+	DC	A(IN39) address of instruction
00001BAC	00001BD6			1712+	DC	A(IN39+6) address of v2 source
00001BB0	00001BE6			1713+	DC	A(IN39+22) address of v3 source
00001BB4	00001BF6			1714+	DC	A(IN39+38) address of v4
				1715+*		
00001BB8				1716+X39	DS	0F
00001BB8	7FE5D4C1 D3404040			1717+CMF39	DC	CL24' "VMAL V1, V2, V3, V4, 0"
00001BC0	E5F16BE5 F26BE5F3					
00001BC8	6BE5F46B F07F4040					
00001BD0				1718+IN39	DC	0F zvector instruction for performance test
00001BD0				1719+	DROP	R5
00001BD0	E712 3000 40AA			1720	VMAL	V1, V2, V3, v4, 0
00001BD6	FF020304 05060708			1721	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v2
00001BDE	090A0B0C 0D0E0F10					
00001BE6	FF020304 05060708			1722	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v3
00001BEE	090A0B0C 0D0E0F10					
00001BF6	FF020304 05060708			1723	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v4
00001BFE	090A0B0C 0D0E0F10					
				1724		
				1725 *		
				1726 * E7AB VMAH		- Vector Multiply and Add High
				1727 *		
				1728		
				1729	PTEST	' "VMAH V1, V2, V3, V4, 0"
00001C08				1730+	DS	0FD
00001C08		00001C08		1731+	USING	*, R5 base for test data and test routine
00001C08	00001C28			1732+T40	DC	A(X40) address of test routine
00001C0C	0028			1733+	DC	H' 40' test number
00001C0E	0000			1734+	DC	H' 00'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001C10	0018			1735+	DC	H' 24'	length of comment
00001C14	00001C28			1736+	DC	A(CMT40)	address of comment
00001C18	00001C40			1737+	DC	A(IN40)	address of instruction
00001C1C	00001C46			1738+	DC	A(IN40+6)	address of v2 source
00001C20	00001C56			1739+	DC	A(IN40+22)	address of v3 source
00001C24	00001C66			1740+	DC	A(IN40+38)	address of v4
				1741+*			
00001C28				1742+X40	DS	0F	
00001C28	7FE5D4C1 C8404040			1743+CMT40	DC	CL24' "VMAH V1, V2, V3, V4, 0"	
00001C30	E5F16BE5 F26BE5F3						
00001C38	6BE5F46B F07F4040						
00001C40				1744+IN40	DC	0F	zvector instruction for performance test
00001C40				1745+	DROP	R5	
00001C40	E712 3000 40AB			1746	VMAH	V1, V2, V3, v4, 0	
00001C46	FF020304 05060708			1747	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
00001C4E	090A0B0C 0D0E0F10						
00001C56	FF020304 05060708			1748	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
00001C5E	090A0B0C 0D0E0F10						
00001C66	FF020304 05060708			1749	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
00001C6E	090A0B0C 0D0E0F10						
				1750			
				1751 *			
				1752 *	E7AC VMALE	- Vector Multiply and Add Logical Even	
				1753 *			
				1754			
				1755	PTEST	' "VMALE V1, V2, V3, V4, 0"	
00001C78				1756+	DS	0FD	
00001C78		00001C78		1757+	USING	*, R5	base for test data and test routine
00001C78	00001C98			1758+T41	DC	A(X41)	address of test routine
00001C7C	0029			1759+	DC	H' 41'	test number
00001C7E	0000			1760+	DC	H' 00'	
00001C80	0018			1761+	DC	H' 24'	length of comment
00001C84	00001C98			1762+	DC	A(CMT41)	address of comment
00001C88	00001CB0			1763+	DC	A(IN41)	address of instruction
00001C8C	00001CB6			1764+	DC	A(IN41+6)	address of v2 source
00001C90	00001CC6			1765+	DC	A(IN41+22)	address of v3 source
00001C94	00001CD6			1766+	DC	A(IN41+38)	address of v4
				1767+*			
00001C98				1768+X41	DS	0F	
00001C98	7FE5D4C1 D3C54040			1769+CMT41	DC	CL24' "VMALE V1, V2, V3, V4, 0"	
00001CA0	E5F16BE5 F26BE5F3						
00001CA8	6BE5F46B F07F4040						
00001CB0				1770+IN41	DC	0F	zvector instruction for performance test
00001CB0				1771+	DROP	R5	
00001CB0	E712 3000 40AC			1772	VMALE	V1, V2, V3, v4, 0	
00001CB6	FF020304 05060708			1773	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
00001CBE	090A0B0C 0D0E0F10						
00001CC6	FF020304 05060708			1774	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
00001CCE	090A0B0C 0D0E0F10						
00001CD6	FF020304 05060708			1775	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
00001CDE	090A0B0C 0D0E0F10						
				1776			
				1777 *			
				1778 *	E7AD VMAL0	- Vector Multiply and Add Logical Odd	
				1779 *			
				1780			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001CE8				1781	PTEST	' "VMALE V1, V2, V3, V4, 0"'
00001CE8				1782+	DS	0FD
00001CE8		00001CE8		1783+	USING	*, R5
00001CE8	00001D08			1784+T42	DC	A(X42)
00001CEC	002A			1785+	DC	H' 42'
00001CEE	0000			1786+	DC	H' 00'
00001CF0	0018			1787+	DC	H' 24'
00001CF4	00001D08			1788+	DC	A(CMF42)
00001CF8	00001D20			1789+	DC	A(IN42)
00001CFC	00001D26			1790+	DC	A(IN42+6)
00001D00	00001D36			1791+	DC	A(IN42+22)
00001D04	00001D46			1792+	DC	A(IN42+38)
				1793+*		
00001D08				1794+X42	DS	0F
00001D08	7FE5D4C1 D3C54040			1795+CMF42	DC	CL24' "VMALE V1, V2, V3, V4, 0"'
00001D10	E5F16BE5 F26BE5F3					
00001D18	6BE5F46B F07F4040					
00001D20				1796+IN42	DC	0F
00001D20				1797+	DROP	R5
00001D20	E712 3000 40AC			1798	VMALE	V1, V2, V3, v4, 0
00001D26	FF020304 05060708			1799	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v2
00001D2E	090A0B0C 0D0E0F10					
00001D36	FF020304 05060708			1800	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v3
00001D3E	090A0B0C 0D0E0F10					
00001D46	FF020304 05060708			1801	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v4
00001D4E	090A0B0C 0D0E0F10					
				1802		
				1803 *		
				1804 *	E7AE VMAE	- Vector Multiply and Add Even
				1805 *		
				1806		
00001D58				1807	PTEST	' "VMAE V1, V2, V3, V4, 0"'
00001D58				1808+	DS	0FD
00001D58		00001D58		1809+	USING	*, R5
00001D58	00001D78			1810+T43	DC	A(X43)
00001D5C	002B			1811+	DC	H' 43'
00001D5E	0000			1812+	DC	H' 00'
00001D60	0018			1813+	DC	H' 24'
00001D64	00001D78			1814+	DC	A(CMF43)
00001D68	00001D90			1815+	DC	A(IN43)
00001D6C	00001D96			1816+	DC	A(IN43+6)
00001D70	00001DA6			1817+	DC	A(IN43+22)
00001D74	00001DB6			1818+	DC	A(IN43+38)
				1819+*		
00001D78				1820+X43	DS	0F
00001D78	7FE5D4C1 C5404040			1821+CMF43	DC	CL24' "VMAE V1, V2, V3, V4, 0"'
00001D80	E5F16BE5 F26BE5F3					
00001D88	6BE5F46B F07F4040					
00001D90				1822+IN43	DC	0F
00001D90				1823+	DROP	R5
00001D90	E712 3000 40AE			1824	VMAE	V1, V2, V3, v4, 0
00001D96	FF020304 05060708			1825	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v2
00001D9E	090A0B0C 0D0E0F10					
00001DA6	FF020304 05060708			1826	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v3
00001DAE	090A0B0C 0D0E0F10					
00001DB6	FF020304 05060708			1827	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v4

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
00001DBE	090A0B0C 0D0E0F10			1828	
				1829 *	-----
				1830 * E7AF VMA0	- Vector Multiply and Add Odd
				1831 *	-----
				1832	
00001DC8				1833	PTEST ' "VMA0 V1, V2, V3, V4, 0"'
00001DC8		00001DC8		1834+	DS OFD
00001DC8	00001DE8			1835+	USING *, R5
00001DCC	002C			1836+T44	DC A(X44)
00001DCE	0000			1837+	DC H' 44'
00001DD0	0018			1838+	DC H' 00'
00001DD4	00001DE8			1839+	DC H' 24'
00001DD8	00001E00			1840+	DC A(CMT44)
00001DDC	00001E06			1841+	DC A(IN44)
00001DE0	00001E16			1842+	DC A(IN44+6)
00001DE4	00001E26			1843+	DC A(IN44+22)
				1844+	DC A(IN44+38)
				1845+*	
00001DE8				1846+X44	DS OF
00001DE8	7FE5D4C1 D6404040			1847+CMT44	DC CL24' "VMA0 V1, V2, V3, V4, 0"'
00001DF0	E5F16BE5 F26BE5F3				
00001DF8	6BE5F46B F07F4040				
00001E00				1848+IN44	DC OF
00001E00				1849+	DROP R5
00001E00	E712 3000 40AF			1850	VMA0 V1, V2, V3, v4, 0
00001E06	FF020304 05060708			1851	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v2
00001E0E	090A0B0C 0D0E0F10				
00001E16	FF020304 05060708			1852	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v3
00001E1E	090A0B0C 0D0E0F10				
00001E26	FF020304 05060708			1853	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v4
00001E2E	090A0B0C 0D0E0F10				
				1854	
				1855 *	-----
				1856 * E7B4 VGFM	- Vector Galois Field Multiply Sum
				1857 *	-----
				1858	
00001E38				1859	PTEST ' "VGFM V1, V2, V3, 0"'
00001E38		00001E38		1860+	DS OFD
00001E38	00001E58			1861+	USING *, R5
00001E3C	002D			1862+T45	DC A(X45)
00001E3E	0000			1863+	DC H' 45'
00001E40	0015			1864+	DC H' 00'
00001E44	00001E58			1865+	DC H' 21'
00001E48	00001E70			1866+	DC A(CMT45)
00001E4C	00001E76			1867+	DC A(IN45)
00001E50	00001E86			1868+	DC A(IN45+6)
00001E54	00001E96			1869+	DC A(IN45+22)
				1870+	DC A(IN45+38)
				1871+*	
00001E58				1872+X45	DS OF
00001E58	7FE5C7C6 D4404040			1873+CMT45	DC CL24' "VGFM V1, V2, V3, 0"'
00001E60	E5F16BE5 F26BE5F3				
00001E68	6BF07F40 40404040				
00001E70				1874+IN45	DC OF
00001E70				1875+	DROP R5

zvector instruction for performance test

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001E70	E712 3000 00B4			1876	VGFM	V1, V2, V3, 0		
00001E76	FF020304 05060708			1877	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2	
00001E7E	090A0B0C 0D0E0F10							
00001E86	FF020304 05060708			1878	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3	
00001E8E	090A0B0C 0D0E0F10							
00001E96	FF020304 05060708			1879	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4	
00001E9E	090A0B0C 0D0E0F10							
				1880				
				1881	*	-----		
				1882	*	E7BC VGFM - Vector Galois Field Multiply Sum and Accumulate		
				1883	*	-----		
				1884				
00001EA8				1885	PTEST	' "VGFM V1, V2, V3, V4, 0"'		
00001EA8		00001EA8		1886+	DS	0FD		
00001EA8	00001EC8			1887+	USING	*, R5	base for test data and test routine	
00001EAC	002E			1888+T46	DC	A(X46)	address of test routine	
00001EAE	0000			1889+	DC	H' 46'	test number	
00001EB0	0018			1890+	DC	H' 00'		
00001EB4	00001EC8			1891+	DC	H' 24'	length of comment	
00001EB8	00001EE0			1892+	DC	A(CMT46)	address of comment	
00001EBC	00001EE6			1893+	DC	A(IN46)	address of instruction	
00001EC0	00001EF6			1894+	DC	A(IN46+6)	address of v2 source	
00001EC4	00001F06			1895+	DC	A(IN46+22)	address of v3 source	
				1896+	DC	A(IN46+38)	address of v4	
				1897+*				
00001EC8				1898+X46	DS	0F		
00001EC8	7FE5C7C6 D4C14040			1899+CMT46	DC	CL24' "VGFM V1, V2, V3, V4, 0"'		
00001ED0	E5F16BE5 F26BE5F3							
00001ED8	6BE5F46B F07F4040							
00001EE0				1900+IN46	DC	0F	zvector instruction for performance test	
00001EE0				1901+	DROP	R5		
00001EE0	E712 3000 40BC			1902	VGFM	V1, V2, V3, V4, 0		
00001EE6	FF020304 05060708			1903	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2	
00001EEE	090A0B0C 0D0E0F10							
00001EF6	FF020304 05060708			1904	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3	
00001EFE	090A0B0C 0D0E0F10							
00001F06	FF020304 05060708			1905	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4	
00001F0E	090A0B0C 0D0E0F10							
				1906				
				1907	*	-----		
				1908	*	E7D4 VUPLL - Vector Unpack Logical Low		
				1909	*	-----		
				1910				
				1911	PTEST	' "VUPLL V1, V2, 0"'		
00001F18				1912+	DS	0FD		
00001F18		00001F18		1913+	USING	*, R5	base for test data and test routine	
00001F18	00001F38			1914+T47	DC	A(X47)	address of test routine	
00001F1C	002F			1915+	DC	H' 47'	test number	
00001F1E	0000			1916+	DC	H' 00'		
00001F20	0012			1917+	DC	H' 18'	length of comment	
00001F24	00001F38			1918+	DC	A(CMT47)	address of comment	
00001F28	00001F50			1919+	DC	A(IN47)	address of instruction	
00001F2C	00001F56			1920+	DC	A(IN47+6)	address of v2 source	
00001F30	00001F66			1921+	DC	A(IN47+22)	address of v3 source	
00001F34	00001F76			1922+	DC	A(IN47+38)	address of v4	
				1923+*				

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001F38				1924+X47	DS	0F
00001F38	7FE5E4D7 D3D34040			1925+CMF47	DC	CL24' "VUPLL V1, V2, 0"
00001F40	E5F16BE5 F26BF07F					
00001F48	40404040 40404040					
00001F50				1926+IN47	DC	0F zvector instruction for performance test
00001F50				1927+	DROP	R5
00001F50	E712 0000 00D4			1928	VUPLL	V1, V2, 0
00001F56	FF020304 05060708			1929	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v2
00001F5E	090A0B0C 0D0E0F10					
00001F66	FF020304 05060708			1930	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v3
00001F6E	090A0B0C 0D0E0F10					
00001F76	FF020304 05060708			1931	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v4
00001F7E	090A0B0C 0D0E0F10					
				1932		
				1933 *		
				1934 * E7D5 VUPLH		- Vector Unpack Logical High
				1935 *		
				1936		
00001F88				1937	PTEST	' "VUPLH V1, V2, 0"
00001F88		00001F88		1938+	DS	0FD
00001F88	00001FA8			1939+	USING	*, R5 base for test data and test routine
00001F8C	0030			1940+T48	DC	A(X48) address of test routine
00001F8E	0000			1941+	DC	H' 48' test number
00001F90	0012			1942+	DC	H' 00'
00001F94	00001FA8			1943+	DC	H' 18' length of comment
00001F98	00001FC0			1944+	DC	A(CMF48) address of comment
00001F9C	00001FC6			1945+	DC	A(IN48) address of instruction
00001FA0	00001FD6			1946+	DC	A(IN48+6) address of v2 source
00001FA4	00001FE6			1947+	DC	A(IN48+22) address of v3 source
				1948+	DC	A(IN48+38) address of v4
				1949+*		
00001FA8				1950+X48	DS	0F
00001FA8	7FE5E4D7 D3C84040			1951+CMF48	DC	CL24' "VUPLH V1, V2, 0"
00001FB0	E5F16BE5 F26BF07F					
00001FB8	40404040 40404040					
00001FC0				1952+IN48	DC	0F zvector instruction for performance test
00001FC0				1953+	DROP	R5
00001FC0	E712 0000 00D5			1954	VUPLH	V1, V2, 0
00001FC6	FF020304 05060708			1955	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v2
00001FCE	090A0B0C 0D0E0F10					
00001FD6	FF020304 05060708			1956	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v3
00001FDE	090A0B0C 0D0E0F10					
00001FE6	FF020304 05060708			1957	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v4
00001FEE	090A0B0C 0D0E0F10					
				1958		
				1959 *		
				1960 * E7D6 VUPL		- Vector Unpack Low
				1961 *		
				1962		
				1963	PTEST	' "VUPL V1, V2, 0"
00001FF8				1964+	DS	0FD
00001FF8		00001FF8		1965+	USING	*, R5 base for test data and test routine
00001FF8	00002018			1966+T49	DC	A(X49) address of test routine
00001FFC	0031			1967+	DC	H' 49' test number
00001FFE	0000			1968+	DC	H' 00'
00002000	0012			1969+	DC	H' 18' length of comment

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002004	00002018			1970+	DC	A(CMT49)	address of comment
00002008	00002030			1971+	DC	A(IN49)	address of instruction
0000200C	00002036			1972+	DC	A(IN49+6)	address of v2 source
00002010	00002046			1973+	DC	A(IN49+22)	address of v3 source
00002014	00002056			1974+	DC	A(IN49+38)	address of v4
				1975+*			
00002018				1976+X49	DS	0F	
00002018	7FE5E4D7 D3404040			1977+CMT49	DC	CL24' "VUPL V1, V2, 0"	
00002020	E5F16BE5 F26BF07F						
00002028	40404040 40404040						
00002030				1978+IN49	DC	0F	zvector instruction for performance test
00002030				1979+	DROP	R5	
00002030	E712 0000 00D6			1980	VUPL	V1, V2, 0	
00002036	FF020304 05060708			1981	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
0000203E	090A0B0C 0D0E0F10						
00002046	FF020304 05060708			1982	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
0000204E	090A0B0C 0D0E0F10						
00002056	FF020304 05060708			1983	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
0000205E	090A0B0C 0D0E0F10						
				1984			
				1985 *			
				1986 *	E7D7 VUPH	- Vector Unpack High	
				1987 *			
				1988			
00002068				1989	PTEST	' "VUPH V1, V2, 0"	
00002068		00002068		1990+	DS	0FD	
00002068	00002088			1991+	USING	*, R5	base for test data and test routine
0000206C	0032			1992+T50	DC	A(X50)	address of test routine
0000206E	0000			1993+	DC	H' 50'	test number
00002070	0012			1994+	DC	H' 00'	
00002074	00002088			1995+	DC	H' 18'	length of comment
00002078	000020A0			1996+	DC	A(CMT50)	address of comment
0000207C	000020A6			1997+	DC	A(IN50)	address of instruction
00002080	000020B6			1998+	DC	A(IN50+6)	address of v2 source
00002084	000020C6			1999+	DC	A(IN50+22)	address of v3 source
				2000+	DC	A(IN50+38)	address of v4
				2001+*			
00002088				2002+X50	DS	0F	
00002088	7FE5E4D7 C8404040			2003+CMT50	DC	CL24' "VUPH V1, V2, 0"	
00002090	E5F16BE5 F26BF07F						
00002098	40404040 40404040						
000020A0				2004+IN50	DC	0F	zvector instruction for performance test
000020A0				2005+	DROP	R5	
000020A0	E712 0000 00D7			2006	VUPH	V1, V2, 0	
000020A6	FF020304 05060708			2007	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
000020AE	090A0B0C 0D0E0F10						
000020B6	FF020304 05060708			2008	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
000020BE	090A0B0C 0D0E0F10						
000020C6	FF020304 05060708			2009	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
000020CE	090A0B0C 0D0E0F10						
				2010			
				2011 *			
				2012 *	E7DE VLC	- Vector Load Complement	
				2013 *			
				2014			
				2015	PTEST	' "VLC V1, V2, 0"	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000020D8				2016+	DS	OFD	
000020D8		000020D8		2017+	USING	*, R5	base for test data and test routine
000020D8	000020F8			2018+T51	DC	A(X51)	address of test routine
000020DC	0033			2019+	DC	H' 51'	test number
000020DE	0000			2020+	DC	H' 00'	
000020E0	0012			2021+	DC	H' 18'	length of comment
000020E4	000020F8			2022+	DC	A(CMT51)	address of comment
000020E8	00002110			2023+	DC	A(IN51)	address of instruction
000020EC	00002116			2024+	DC	A(IN51+6)	address of v2 source
000020F0	00002126			2025+	DC	A(IN51+22)	address of v3 source
000020F4	00002136			2026+	DC	A(IN51+38)	address of v4
				2027+*			
000020F8				2028+X51	DS	0F	
000020F8	7FE5D3C3 40404040			2029+CMT51	DC	CL24' "VLC V1, V2, 0"'	
00002100	E5F16BE5 F26BF07F						
00002108	40404040 40404040						
00002110				2030+IN51	DC	0F	zvector instruction for performance test
00002110				2031+	DROP	R5	
00002110	E712 0000 00DE			2032	VLC	V1, V2, 0	
00002116	FF020304 05060708			2033	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
0000211E	090A0B0C 0D0E0F10						
00002126	FF020304 05060708			2034	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
0000212E	090A0B0C 0D0E0F10						
00002136	FF020304 05060708			2035	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
0000213E	090A0B0C 0D0E0F10						
				2036			
				2037 *			
				2038 * E7DF VLP		- Vector Load Positive	
				2039 *			
				2040			
				2041	PTEST	' "VLP V1, V2, 0"'	
00002148				2042+	DS	OFD	
00002148		00002148		2043+	USING	*, R5	base for test data and test routine
00002148	00002168			2044+T52	DC	A(X52)	address of test routine
0000214C	0034			2045+	DC	H' 52'	test number
0000214E	0000			2046+	DC	H' 00'	
00002150	0012			2047+	DC	H' 18'	length of comment
00002154	00002168			2048+	DC	A(CMT52)	address of comment
00002158	00002180			2049+	DC	A(IN52)	address of instruction
0000215C	00002186			2050+	DC	A(IN52+6)	address of v2 source
00002160	00002196			2051+	DC	A(IN52+22)	address of v3 source
00002164	000021A6			2052+	DC	A(IN52+38)	address of v4
				2053+*			
00002168				2054+X52	DS	0F	
00002168	7FE5D3D7 40404040			2055+CMT52	DC	CL24' "VLP V1, V2, 0"'	
00002170	E5F16BE5 F26BF07F						
00002178	40404040 40404040						
00002180				2056+IN52	DC	0F	zvector instruction for performance test
00002180				2057+	DROP	R5	
00002180	E712 0000 00DF			2058	VLP	V1, V2, 0	
00002186	FF020304 05060708			2059	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
0000218E	090A0B0C 0D0E0F10						
00002196	FF020304 05060708			2060	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
0000219E	090A0B0C 0D0E0F10						
000021A6	FF020304 05060708			2061	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
000021AE	090A0B0C 0D0E0F10						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				2062	
				2063 *	-----
				2064 *	E7F0 VAVGL - Vector Average Logical
				2065 *	-----
				2066	
000021B8				2067	PTEST ' "VAVGL V1, V2, V3, 0"'
000021B8		000021B8		2068+	DS OFD
000021B8	000021D8			2069+	USING *, R5 base for test data and test routine
000021BC	0035			2070+T53	DC A(X53) address of test routine
000021BE	0000			2071+	DC H' 53' test number
000021C0	0015			2072+	DC H' 00'
000021C4	000021D8			2073+	DC H' 21' length of comment
000021C8	000021F0			2074+	DC A(CMT53) address of comment
000021CC	000021F6			2075+	DC A(IN53) address of instruction
000021D0	00002206			2076+	DC A(IN53+6) address of v2 source
000021D4	00002216			2077+	DC A(IN53+22) address of v3 source
				2078+	DC A(IN53+38) address of v4
				2079+*	
000021D8				2080+X53	DS OF
000021D8	7FE5C1E5 C7D34040			2081+CMT53	DC CL24' "VAVGL V1, V2, V3, 0"'
000021E0	E5F16BE5 F26BE5F3				
000021E8	6BF07F40 40404040				
000021F0				2082+IN53	DC OF zvector instruction for performance test
000021F0				2083+	DROP R5
000021F0	E712 3000 00F0			2084	VAVGL V1, V2, V3, 0
000021F6	FF020304 05060708			2085	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v2
000021FE	090A0B0C 0D0E0F10				
00002206	FF020304 05060708			2086	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v3
0000220E	090A0B0C 0D0E0F10				
00002216	FF020304 05060708			2087	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v4
0000221E	090A0B0C 0D0E0F10				
				2088	
				2089 *	-----
				2090 *	E7F2 VAVG - Vector Average
				2091 *	-----
				2092	
00002228				2093	PTEST ' "VAVG V1, V2, V3, 0"'
00002228		00002228		2094+	DS OFD
00002228	00002248			2095+	USING *, R5 base for test data and test routine
0000222C	0036			2096+T54	DC A(X54) address of test routine
0000222E	0000			2097+	DC H' 54' test number
00002230	0015			2098+	DC H' 00'
00002234	00002248			2099+	DC H' 21' length of comment
00002238	00002260			2100+	DC A(CMT54) address of comment
0000223C	00002266			2101+	DC A(IN54) address of instruction
00002240	00002276			2102+	DC A(IN54+6) address of v2 source
00002244	00002286			2103+	DC A(IN54+22) address of v3 source
				2104+	DC A(IN54+38) address of v4
				2105+*	
00002248				2106+X54	DS OF
00002248	7FE5C1E5 C7404040			2107+CMT54	DC CL24' "VAVG V1, V2, V3, 0"'
00002250	E5F16BE5 F26BE5F3				
00002258	6BF07F40 40404040				
00002260				2108+IN54	DC OF zvector instruction for performance test
00002260				2109+	DROP R5
00002260	E712 3000 00F2			2110	VAVG V1, V2, V3, 0

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002266	FF020304 05060708			2111	DC	XL16'	FF02030405060708 090A0B0C0D0E0F10'	v2
0000226E	090A0B0C 0D0E0F10							
00002276	FF020304 05060708			2112	DC	XL16'	FF02030405060708 090A0B0C0D0E0F10'	v3
0000227E	090A0B0C 0D0E0F10							
00002286	FF020304 05060708			2113	DC	XL16'	FF02030405060708 090A0B0C0D0E0F10'	v4
0000228E	090A0B0C 0D0E0F10							
				2114				
				2115	*	-----		
				2116	*	E7F3 VA	- Vector Add	
				2117	*	-----		
				2118				
00002298				2119	PTEST	' "VA	V1, V2, V3, 0"	
00002298		00002298		2120+	DS	0FD		
00002298	000022B8			2121+	USING	*, R5		base for test data and test routine
0000229C	0037			2122+T55	DC	A(X55)		address of test routine
0000229E	0000			2123+	DC	H' 55'		test number
000022A0	0015			2124+	DC	H' 00'		
000022A4	000022B8			2125+	DC	H' 21'		length of comment
000022A8	000022D0			2126+	DC	A(CMF55)		address of comment
000022AC	000022D6			2127+	DC	A(IN55)		address of instruction
000022B0	000022E6			2128+	DC	A(IN55+6)		address of v2 source
000022B4	000022F6			2129+	DC	A(IN55+22)		address of v3 source
				2130+	DC	A(IN55+38)		address of v4
				2131+*				
000022B8				2132+X55	DS	0F		
000022B8	7FE5C140 40404040			2133+CMF55	DC	CL24'	"VA V1, V2, V3, 0"	
000022C0	E5F16BE5 F26BE5F3							
000022C8	6BF07F40 40404040							
000022D0				2134+IN55	DC	0F		zvector instruction for performance test
000022D0				2135+	DROP	R5		
000022D0	E712 3000 00F3			2136	VA	V1, V2, V3, 0		
000022D6	FF020304 05060708			2137	DC	XL16'	FF02030405060708 090A0B0C0D0E0F10'	v2
000022DE	090A0B0C 0D0E0F10							
000022E6	FF020304 05060708			2138	DC	XL16'	FF02030405060708 090A0B0C0D0E0F10'	v3
000022EE	090A0B0C 0D0E0F10							
000022F6	FF020304 05060708			2139	DC	XL16'	FF02030405060708 090A0B0C0D0E0F10'	v4
000022FE	090A0B0C 0D0E0F10							
				2140				
				2141	*	-----		
				2142	*	E7F5 VSCBI	- Vector Subtract Compute Borrow Indication	
				2143	*	-----		
				2144				
00002308				2145	PTEST	' "VSCBI	V1, V2, V3, 0"	
00002308		00002308		2146+	DS	0FD		
00002308	00002328			2147+	USING	*, R5		base for test data and test routine
0000230C	0038			2148+T56	DC	A(X56)		address of test routine
0000230E	0000			2149+	DC	H' 56'		test number
00002310	0015			2150+	DC	H' 00'		
00002314	00002328			2151+	DC	H' 21'		length of comment
00002318	00002340			2152+	DC	A(CMF56)		address of comment
0000231C	00002346			2153+	DC	A(IN56)		address of instruction
00002320	00002356			2154+	DC	A(IN56+6)		address of v2 source
00002324	00002366			2155+	DC	A(IN56+22)		address of v3 source
				2156+	DC	A(IN56+38)		address of v4
				2157+*				
00002328				2158+X56	DS	0F		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00002328	7FE5E2C3 C2C94040			2159+CMF56	DC	CL24' "VSCBI V1, V2, V3, 0"
00002330	E5F16BE5 F26BE5F3					
00002338	6BF07F40 40404040					
00002340				2160+IN56	DC	OF zvector instruction for performance test
00002340				2161+	DROP	R5
00002340	E712 3000 00F5			2162	VSCBI	V1, V2, V3, 0
00002346	FF020304 05060708			2163	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v2
0000234E	090A0B0C 0D0E0F10					
00002356	FF020304 05060708			2164	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v3
0000235E	090A0B0C 0D0E0F10					
00002366	FF020304 05060708			2165	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v4
0000236E	090A0B0C 0D0E0F10					
				2166		
				2167 *		
				2168 * E7F7 VS		- Vector Subtract
				2169 *		
				2170		
00002378				2171	PTEST	' "VS V1, V2, V3, 0"
00002378		00002378		2172+	DS	OFD
00002378	00002398			2173+	USING	*, R5
0000237C	0039			2174+T57	DC	A(X57)
0000237E	0000			2175+	DC	H' 57'
00002380	0015			2176+	DC	H' 00'
00002384	00002398			2177+	DC	H' 21'
00002388	000023B0			2178+	DC	A(CMF57)
0000238C	000023B6			2179+	DC	A(IN57)
00002390	000023C6			2180+	DC	A(IN57+6)
00002394	000023D6			2181+	DC	A(IN57+22)
				2182+	DC	A(IN57+38)
				2183+*		
00002398				2184+X57	DS	OF
00002398	7FE5E240 40404040			2185+CMF57	DC	CL24' "VS V1, V2, V3, 0"
000023A0	E5F16BE5 F26BE5F3					
000023A8	6BF07F40 40404040					
000023B0				2186+IN57	DC	OF zvector instruction for performance test
000023B0				2187+	DROP	R5
000023B0	E712 3000 00F7			2188	VS	V1, V2, V3, 0
000023B6	FF020304 05060708			2189	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v2
000023BE	090A0B0C 0D0E0F10					
000023C6	FF020304 05060708			2190	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v3
000023CE	090A0B0C 0D0E0F10					
000023D6	FF020304 05060708			2191	DC	XL16' FF02030405060708 090A0B0C0D0E0F10' v4
000023DE	090A0B0C 0D0E0F10					
				2192		
				2193 *		
				2194 * E7F8 VCEQ		- Vector Compare Equal
				2195 *		
				2196		
000023E8				2197	PTEST	' "VCEQ V1, V2, V3, 0, 1"
000023E8		000023E8		2198+	DS	OFD
000023E8	00002408			2199+	USING	*, R5
000023EC	003A			2200+T58	DC	A(X58)
000023EE	0000			2201+	DC	H' 58'
000023F0	0017			2202+	DC	H' 00'
000023F4	00002408			2203+	DC	H' 23'
				2204+	DC	A(CMF58)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000023F8	00002420			2205+	DC	A(IN58)	address of instruction
000023FC	00002426			2206+	DC	A(IN58+6)	address of v2 source
00002400	00002436			2207+	DC	A(IN58+22)	address of v3 source
00002404	00002446			2208+	DC	A(IN58+38)	address of v4
				2209+*			
00002408				2210+X58	DS	0F	
00002408	7FE5C3C5 D8404040			2211+CMF58	DC	CL24' "VCEQ V1, V2, V3, 0, 1"	
00002410	E5F16BE5 F26BE5F3						
00002418	6BF06BF1 7F404040						
00002420				2212+IN58	DC	0F	zvector instruction for performance test
00002420				2213+	DROP	R5	
00002420	E712 3010 00F8			2214	VCEQ	V1, V2, V3, 0, 1	
00002426	FF020304 05060708			2215	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
0000242E	090A0B0C 0D0E0F10						
00002436	FF020304 05060708			2216	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
0000243E	090A0B0C 0D0E0F10						
00002446	FF020304 05060708			2217	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
0000244E	090A0B0C 0D0E0F10						
				2218			
				2219 *			
				2220 *	E7F9 VCHL	- Vector Compare High Logical	
				2221 *			
				2222			
				2223	PTEST	' "VCHL V1, V2, V3, 0, 1"	
00002458				2224+	DS	0FD	
00002458		00002458		2225+	USING	*, R5	base for test data and test routine
00002458	00002478			2226+T59	DC	A(X59)	address of test routine
0000245C	003B			2227+	DC	H' 59'	test number
0000245E	0000			2228+	DC	H' 00'	
00002460	0017			2229+	DC	H' 23'	length of comment
00002464	00002478			2230+	DC	A(CMF59)	address of comment
00002468	00002490			2231+	DC	A(IN59)	address of instruction
0000246C	00002496			2232+	DC	A(IN59+6)	address of v2 source
00002470	000024A6			2233+	DC	A(IN59+22)	address of v3 source
00002474	000024B6			2234+	DC	A(IN59+38)	address of v4
				2235+*			
00002478				2236+X59	DS	0F	
00002478	7FE5C3C8 D3404040			2237+CMF59	DC	CL24' "VCHL V1, V2, V3, 0, 1"	
00002480	E5F16BE5 F26BE5F3						
00002488	6BF06BF1 7F404040						
00002490				2238+IN59	DC	0F	zvector instruction for performance test
00002490				2239+	DROP	R5	
00002490	E712 3010 00F9			2240	VCHL	V1, V2, V3, 0, 1	
00002496	FF020304 05060708			2241	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
0000249E	090A0B0C 0D0E0F10						
000024A6	FF020304 05060708			2242	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
000024AE	090A0B0C 0D0E0F10						
000024B6	FF020304 05060708			2243	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
000024BE	090A0B0C 0D0E0F10						
				2244			
				2245 *			
				2246 *	E7FB VCH	- Vector Compare High	
				2247 *			
				2248			
				2249	PTEST	' "VCH V1, V2, V3, 0, 1"	
000024C8				2250+	DS	0FD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000024C8		000024C8		2251+	USING *, R5	base for test data and test routine
000024C8	000024E8			2252+T60	DC A(X60)	address of test routine
000024CC	003C			2253+	DC H' 60'	test number
000024CE	0000			2254+	DC H' 00'	
000024D0	0017			2255+	DC H' 23'	length of comment
000024D4	000024E8			2256+	DC A(CMT60)	address of comment
000024D8	00002500			2257+	DC A(IN60)	address of instruction
000024DC	00002506			2258+	DC A(IN60+6)	address of v2 source
000024E0	00002516			2259+	DC A(IN60+22)	address of v3 source
000024E4	00002526			2260+	DC A(IN60+38)	address of v4
				2261+*		
000024E8				2262+X60	DS 0F	
000024E8	7FE5C3C8 40404040			2263+CMT60	DC CL24' "VCH V1, V2, V3, 0, 1"	
000024F0	E5F16BE5 F26BE5F3					
000024F8	6BF06BF1 7F404040					
00002500				2264+IN60	DC 0F	zvector instruction for performance test
00002500				2265+	DROP R5	
00002500	E712 3010 00FB			2266	VCH V1, V2, V3, 0, 1	
00002506	FF020304 05060708			2267	DC XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
0000250E	090A0B0C 0D0E0F10					
00002516	FF020304 05060708			2268	DC XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
0000251E	090A0B0C 0D0E0F10					
00002526	FF020304 05060708			2269	DC XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
0000252E	090A0B0C 0D0E0F10					
				2270		
				2271 *	-----	
				2272 *	E7FC VMNL - Vector Minimum Logical	
				2273 *	-----	
				2274		
				2275	PTEST ' "VMNL V1, V2, V3, 0"	
00002538				2276+	DS 0FD	
00002538		00002538		2277+	USING *, R5	base for test data and test routine
00002538	00002558			2278+T61	DC A(X61)	address of test routine
0000253C	003D			2279+	DC H' 61'	test number
0000253E	0000			2280+	DC H' 00'	
00002540	0015			2281+	DC H' 21'	length of comment
00002544	00002558			2282+	DC A(CMT61)	address of comment
00002548	00002570			2283+	DC A(IN61)	address of instruction
0000254C	00002576			2284+	DC A(IN61+6)	address of v2 source
00002550	00002586			2285+	DC A(IN61+22)	address of v3 source
00002554	00002596			2286+	DC A(IN61+38)	address of v4
				2287+*		
00002558				2288+X61	DS 0F	
00002558	7FE5D4D5 D3404040			2289+CMT61	DC CL24' "VMNL V1, V2, V3, 0"	
00002560	E5F16BE5 F26BE5F3					
00002568	6BF07F40 40404040					
00002570				2290+IN61	DC 0F	zvector instruction for performance test
00002570				2291+	DROP R5	
00002570	E712 3000 00FC			2292	VMNL V1, V2, V3, 0	
00002576	FF020304 05060708			2293	DC XL16' FF02030405060708 090A0B0C0D0E0F10'	v2
0000257E	090A0B0C 0D0E0F10					
00002586	FF020304 05060708			2294	DC XL16' FF02030405060708 090A0B0C0D0E0F10'	v3
0000258E	090A0B0C 0D0E0F10					
00002596	FF020304 05060708			2295	DC XL16' FF02030405060708 090A0B0C0D0E0F10'	v4
0000259E	090A0B0C 0D0E0F10					
				2296		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				2297 *	-----
				2298 *	E7FD VMKL - Vector Maximum Logical
				2299 *	-----
				2300	
				2301	PTEST ' "VMKL V1, V2, V3, 0"'
000025A8				2302+	DS OFD
000025A8		000025A8		2303+	USING *, R5
000025A8	000025C8			2304+T62	DC A(X62)
000025AC	003E			2305+	DC H' 62'
000025AE	0000			2306+	DC H' 00'
000025B0	0015			2307+	DC H' 21'
000025B4	000025C8			2308+	DC A(CMT62)
000025B8	000025E0			2309+	DC A(IN62)
000025BC	000025E6			2310+	DC A(IN62+6)
000025C0	000025F6			2311+	DC A(IN62+22)
000025C4	00002606			2312+	DC A(IN62+38)
				2313+*	
000025C8				2314+X62	DS OF
000025C8	7FE5D4E7 D3404040			2315+CMT62	DC CL24' "VMKL V1, V2, V3, 0"'
000025D0	E5F16BE5 F26BE5F3				
000025D8	6BF07F40 40404040				
000025E0				2316+IN62	DC OF
000025E0				2317+	DROP R5
000025E0	E712 3000 00FD			2318	VMKL V1, V2, V3, 0
000025E6	FF020304 05060708			2319	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v2
000025EE	090A0B0C 0D0E0F10				
000025F6	FF020304 05060708			2320	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v3
000025FE	090A0B0C 0D0E0F10				
00002606	FF020304 05060708			2321	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v4
0000260E	090A0B0C 0D0E0F10				
				2322	
				2323 *	-----
				2324 *	E7FE VMN - Vector Minimum
				2325 *	-----
				2326	
				2327	PTEST ' "VMN V1, V2, V3, 0"'
00002618				2328+	DS OFD
00002618		00002618		2329+	USING *, R5
00002618	00002638			2330+T63	DC A(X63)
0000261C	003F			2331+	DC H' 63'
0000261E	0000			2332+	DC H' 00'
00002620	0015			2333+	DC H' 21'
00002624	00002638			2334+	DC A(CMT63)
00002628	00002650			2335+	DC A(IN63)
0000262C	00002656			2336+	DC A(IN63+6)
00002630	00002666			2337+	DC A(IN63+22)
00002634	00002676			2338+	DC A(IN63+38)
				2339+*	
00002638				2340+X63	DS OF
00002638	7FE5D4D5 40404040			2341+CMT63	DC CL24' "VMN V1, V2, V3, 0"'
00002640	E5F16BE5 F26BE5F3				
00002648	6BF07F40 40404040				
00002650				2342+IN63	DC OF
00002650				2343+	DROP R5
00002650	E712 3000 00FE			2344	VMN V1, V2, V3, 0
00002656	FF020304 05060708			2345	DC XL16' FF02030405060708 090A0B0C0D0E0F10' v2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
0000265E	090A0B0C 0D0E0F10							
00002666	FF020304 05060708			2346	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3	
0000266E	090A0B0C 0D0E0F10							
00002676	FF020304 05060708			2347	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4	
0000267E	090A0B0C 0D0E0F10							
				2348				
				2349	*	-----		
				2350	*	E7FF VMK - Vector Maximum		
				2351	*	-----		
				2352				
				2353		PTEST ' "VMK V1, V2, V3, 0"'		
00002688				2354+	DS	0FD		
00002688		00002688		2355+	USING	*, R5		base for test data and test routine
00002688	000026A8			2356+T64	DC	A(X64)		address of test routine
0000268C	0040			2357+	DC	H' 64'		test number
0000268E	0000			2358+	DC	H' 00'		
00002690	0015			2359+	DC	H' 21'		length of comment
00002694	000026A8			2360+	DC	A(CMT64)		address of comment
00002698	000026C0			2361+	DC	A(IN64)		address of instruction
0000269C	000026C6			2362+	DC	A(IN64+6)		address of v2 source
000026A0	000026D6			2363+	DC	A(IN64+22)		address of v3 source
000026A4	000026E6			2364+	DC	A(IN64+38)		address of v4
				2365+*				
000026A8				2366+X64	DS	0F		
000026A8	7FE5D4E7 40404040			2367+CMT64	DC	CL24' "VMK V1, V2, V3, 0"'		
000026B0	E5F16BE5 F26BE5F3							
000026B8	6BF07F40 40404040							
000026C0				2368+IN64	DC	0F		zvector instruction for performance test
000026C0				2369+	DROP	R5		
000026C0	E712 3000 00FF			2370	VMK	V1, V2, V3, 0		
000026C6	FF020304 05060708			2371	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v2	
000026CE	090A0B0C 0D0E0F10							
000026D6	FF020304 05060708			2372	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v3	
000026DE	090A0B0C 0D0E0F10							
000026E6	FF020304 05060708			2373	DC	XL16' FF02030405060708 090A0B0C0D0E0F10'	v4	
000026EE	090A0B0C 0D0E0F10							
				2374				
				2375				
				2376				
				2377				
				2378				
000026F8	00000000			2379	DC	F' 0' END OF TABLE		
000026FC	00000000			2380	DC	F' 0'		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2382 *
				2383 * table of pointers to individual load test
				2384 *
00002700				2385 E7TESTS DS OF
				2386 PTTABLE
00002700				2387+TTABLE DS OF
00002700	00000AF8			2388+ DC A(T1)
00002704	00000B68			2389+ DC A(T2)
00002708	00000BD8			2390+ DC A(T3)
0000270C	00000C48			2391+ DC A(T4)
00002710	00000CB8			2392+ DC A(T5)
00002714	00000D28			2393+ DC A(T6)
00002718	00000D98			2394+ DC A(T7)
0000271C	00000E08			2395+ DC A(T8)
00002720	00000E78			2396+ DC A(T9)
00002724	00000EE8			2397+ DC A(T10)
00002728	00000F58			2398+ DC A(T11)
0000272C	00000FC8			2399+ DC A(T12)
00002730	00001038			2400+ DC A(T13)
00002734	000010A8			2401+ DC A(T14)
00002738	00001118			2402+ DC A(T15)
0000273C	00001188			2403+ DC A(T16)
00002740	000011F8			2404+ DC A(T17)
00002744	00001268			2405+ DC A(T18)
00002748	000012D8			2406+ DC A(T19)
0000274C	00001348			2407+ DC A(T20)
00002750	000013B8			2408+ DC A(T21)
00002754	00001428			2409+ DC A(T22)
00002758	00001498			2410+ DC A(T23)
0000275C	00001508			2411+ DC A(T24)
00002760	00001578			2412+ DC A(T25)
00002764	000015E8			2413+ DC A(T26)
00002768	00001658			2414+ DC A(T27)
0000276C	000016C8			2415+ DC A(T28)
00002770	00001738			2416+ DC A(T29)
00002774	000017A8			2417+ DC A(T30)
00002778	00001818			2418+ DC A(T31)
0000277C	00001888			2419+ DC A(T32)
00002780	000018F8			2420+ DC A(T33)
00002784	00001968			2421+ DC A(T34)
00002788	000019D8			2422+ DC A(T35)
0000278C	00001A48			2423+ DC A(T36)
00002790	00001AB8			2424+ DC A(T37)
00002794	00001B28			2425+ DC A(T38)
00002798	00001B98			2426+ DC A(T39)
0000279C	00001C08			2427+ DC A(T40)
000027A0	00001C78			2428+ DC A(T41)
000027A4	00001CE8			2429+ DC A(T42)
000027A8	00001D58			2430+ DC A(T43)
000027AC	00001DC8			2431+ DC A(T44)
000027B0	00001E38			2432+ DC A(T45)
000027B4	00001EA8			2433+ DC A(T46)
000027B8	00001F18			2434+ DC A(T47)
000027BC	00001F88			2435+ DC A(T48)
000027C0	00001FF8			2436+ DC A(T49)
000027C4	00002068			2437+ DC A(T50)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				2458	*****	
				2459	* Register equates	
				2460	*****	
		00000000	00000001	2462 R0	EQU	0
		00000001	00000001	2463 R1	EQU	1
		00000002	00000001	2464 R2	EQU	2
		00000003	00000001	2465 R3	EQU	3
		00000004	00000001	2466 R4	EQU	4
		00000005	00000001	2467 R5	EQU	5
		00000006	00000001	2468 R6	EQU	6
		00000007	00000001	2469 R7	EQU	7
		00000008	00000001	2470 R8	EQU	8
		00000009	00000001	2471 R9	EQU	9
		0000000A	00000001	2472 R10	EQU	10
		0000000B	00000001	2473 R11	EQU	11
		0000000C	00000001	2474 R12	EQU	12
		0000000D	00000001	2475 R13	EQU	13
		0000000E	00000001	2476 R14	EQU	14
		0000000F	00000001	2477 R15	EQU	15
				2479	*****	
				2480	* Register equates	
				2481	*****	
		00000000	00000001	2483 V0	EQU	0
		00000001	00000001	2484 V1	EQU	1
		00000002	00000001	2485 V2	EQU	2
		00000003	00000001	2486 V3	EQU	3
		00000004	00000001	2487 V4	EQU	4
		00000005	00000001	2488 V5	EQU	5
		00000006	00000001	2489 V6	EQU	6
		00000007	00000001	2490 V7	EQU	7
		00000008	00000001	2491 V8	EQU	8
		00000009	00000001	2492 V9	EQU	9
		0000000A	00000001	2493 V10	EQU	10
		0000000B	00000001	2494 V11	EQU	11
		0000000C	00000001	2495 V12	EQU	12
		0000000D	00000001	2496 V13	EQU	13
		0000000E	00000001	2497 V14	EQU	14
		0000000F	00000001	2498 V15	EQU	15
		00000010	00000001	2499 V16	EQU	16
		00000011	00000001	2500 V17	EQU	17
		00000012	00000001	2501 V18	EQU	18
		00000013	00000001	2502 V19	EQU	19
		00000014	00000001	2503 V20	EQU	20
		00000015	00000001	2504 V21	EQU	21

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
BEGIN	I	000200	2	165	342 131 161 162 163
CMF1	C	000B18	24	729	722
CMF10	C	000F08	24	963	956
CMF11	C	000F78	24	989	982
CMF12	C	000FE8	24	1015	1008
CMF13	C	001058	24	1041	1034
CMF14	C	0010C8	24	1067	1060
CMF15	C	001138	24	1093	1086
CMF16	C	0011A8	24	1119	1112
CMF17	C	001218	24	1145	1138
CMF18	C	001288	24	1171	1164
CMF19	C	0012F8	24	1197	1190
CMF2	C	000B88	24	755	748
CMF20	C	001368	24	1223	1216
CMF21	C	0013D8	24	1249	1242
CMF22	C	001448	24	1275	1268
CMF23	C	0014B8	24	1301	1294
CMF24	C	001528	24	1327	1320
CMF25	C	001598	24	1353	1346
CMF26	C	001608	24	1379	1372
CMF27	C	001678	24	1405	1398
CMF28	C	0016E8	24	1431	1424
CMF29	C	001758	24	1457	1450
CMF3	C	000BF8	24	781	774
CMF30	C	0017C8	24	1483	1476
CMF31	C	001838	24	1509	1502
CMF32	C	0018A8	24	1535	1528
CMF33	C	001918	24	1561	1554
CMF34	C	001988	24	1587	1580
CMF35	C	0019F8	24	1613	1606
CMF36	C	001A68	24	1639	1632
CMF37	C	001AD8	24	1665	1658
CMF38	C	001B48	24	1691	1684
CMF39	C	001BB8	24	1717	1710
CMF4	C	000C68	24	807	800
CMF40	C	001C28	24	1743	1736
CMF41	C	001C98	24	1769	1762
CMF42	C	001D08	24	1795	1788
CMF43	C	001D78	24	1821	1814
CMF44	C	001DE8	24	1847	1840
CMF45	C	001E58	24	1873	1866
CMF46	C	001EC8	24	1899	1892
CMF47	C	001F38	24	1925	1918
CMF48	C	001FA8	24	1951	1944
CMF49	C	002018	24	1977	1970
CMF5	C	000CD8	24	833	826
CMF50	C	002088	24	2003	1996
CMF51	C	0020F8	24	2029	2022
CMF52	C	002168	24	2055	2048
CMF53	C	0021D8	24	2081	2074
CMF54	C	002248	24	2107	2100
CMF55	C	0022B8	24	2133	2126
CMF56	C	002328	24	2159	2152
CMF57	C	002398	24	2185	2178
CMF58	C	002408	24	2211	2204
CMF59	C	002478	24	2237	2230

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES						
CMF6	C	000D48	24	859	852						
CMF60	C	0024E8	24	2263	2256						
CMF61	C	002558	24	2289	2282						
CMF62	C	0025C8	24	2315	2308						
CMF63	C	002638	24	2341	2334						
CMF64	C	0026A8	24	2367	2360						
CMF7	C	000DB8	24	885	878						
CMF8	C	000E28	24	911	904						
CMF9	C	000E98	24	937	930						
CMFADDR	A	00000C	4	613	459						
CTLRO	F	00097C	4	540	178	179	180	181			
DECNUM	C	000AC2	21	599	448	450	454	456			
DONEXT	U	0007C4	1	436							
DOTEST	F	0004E0	4	319	292						
E7TEST	4	000000	32	608	376						
E7TESTS	F	002700	4	2385	365						
EDITITER	X	000A60	18	587	455						
EDITMS	X	000A92	18	593	467						
EDITTNUM	X	000A34	16	581	449						
EOJ	I	000960	4	530	176	213	246	279	299	327	336
EOJPSW	D	000950	8	528	530						
FAILED	F	000608	4	348							
FAILPSW	D	000968	8	532	534						
FAILTEST	I	000978	4	534	334						
FB0001	F	000288	8	197	201	202	204				
FB0002	F	000338	8	230	234	235	237				
FB0003	F	0003E8	8	263	267	268	270				
IMAGE	1	000000	10256	0							
IN1	F	000B30	4	730	723	724	725	726			
IN10	F	000F20	4	964	957	958	959	960			
IN11	F	000F90	4	990	983	984	985	986			
IN12	F	001000	4	1016	1009	1010	1011	1012			
IN13	F	001070	4	1042	1035	1036	1037	1038			
IN14	F	0010E0	4	1068	1061	1062	1063	1064			
IN15	F	001150	4	1094	1087	1088	1089	1090			
IN16	F	0011C0	4	1120	1113	1114	1115	1116			
IN17	F	001230	4	1146	1139	1140	1141	1142			
IN18	F	0012A0	4	1172	1165	1166	1167	1168			
IN19	F	001310	4	1198	1191	1192	1193	1194			
IN2	F	000BA0	4	756	749	750	751	752			
IN20	F	001380	4	1224	1217	1218	1219	1220			
IN21	F	0013F0	4	1250	1243	1244	1245	1246			
IN22	F	001460	4	1276	1269	1270	1271	1272			
IN23	F	0014D0	4	1302	1295	1296	1297	1298			
IN24	F	001540	4	1328	1321	1322	1323	1324			
IN25	F	0015B0	4	1354	1347	1348	1349	1350			
IN26	F	001620	4	1380	1373	1374	1375	1376			
IN27	F	001690	4	1406	1399	1400	1401	1402			
IN28	F	001700	4	1432	1425	1426	1427	1428			
IN29	F	001770	4	1458	1451	1452	1453	1454			
IN3	F	000C10	4	782	775	776	777	778			
IN30	F	0017E0	4	1484	1477	1478	1479	1480			
IN31	F	001850	4	1510	1503	1504	1505	1506			
IN32	F	0018C0	4	1536	1529	1530	1531	1532			
IN33	F	001930	4	1562	1555	1556	1557	1558			
IN34	F	0019A0	4	1588	1581	1582	1583	1584			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
IN35	F	001A10	4	1614	1607	1608	1609	1610	
IN36	F	001A80	4	1640	1633	1634	1635	1636	
IN37	F	001AF0	4	1666	1659	1660	1661	1662	
IN38	F	001B60	4	1692	1685	1686	1687	1688	
IN39	F	001BD0	4	1718	1711	1712	1713	1714	
IN4	F	000C80	4	808	801	802	803	804	
IN40	F	001C40	4	1744	1737	1738	1739	1740	
IN41	F	001CB0	4	1770	1763	1764	1765	1766	
IN42	F	001D20	4	1796	1789	1790	1791	1792	
IN43	F	001D90	4	1822	1815	1816	1817	1818	
IN44	F	001E00	4	1848	1841	1842	1843	1844	
IN45	F	001E70	4	1874	1867	1868	1869	1870	
IN46	F	001EE0	4	1900	1893	1894	1895	1896	
IN47	F	001F50	4	1926	1919	1920	1921	1922	
IN48	F	001FC0	4	1952	1945	1946	1947	1948	
IN49	F	002030	4	1978	1971	1972	1973	1974	
IN5	F	000CF0	4	834	827	828	829	830	
IN50	F	0020A0	4	2004	1997	1998	1999	2000	
IN51	F	002110	4	2030	2023	2024	2025	2026	
IN52	F	002180	4	2056	2049	2050	2051	2052	
IN53	F	0021F0	4	2082	2075	2076	2077	2078	
IN54	F	002260	4	2108	2101	2102	2103	2104	
IN55	F	0022D0	4	2134	2127	2128	2129	2130	
IN56	F	002340	4	2160	2153	2154	2155	2156	
IN57	F	0023B0	4	2186	2179	2180	2181	2182	
IN58	F	002420	4	2212	2205	2206	2207	2208	
IN59	F	002490	4	2238	2231	2232	2233	2234	
IN6	F	000D60	4	860	853	854	855	856	
IN60	F	002500	4	2264	2257	2258	2259	2260	
IN61	F	002570	4	2290	2283	2284	2285	2286	
IN62	F	0025E0	4	2316	2309	2310	2311	2312	
IN63	F	002650	4	2342	2335	2336	2337	2338	
IN64	F	0026C0	4	2368	2361	2362	2363	2364	
IN7	F	000DD0	4	886	879	880	881	882	
IN8	F	000E40	4	912	905	906	907	908	
IN9	F	000EB0	4	938	931	932	933	934	
INADDR	A	000010	4	614	415				
ITERCNT	F	000604	4	346	395	413	453		
K	U	000400	1	553	554	555	556	557	558
K16	U	004000	1	555					
K32	U	008000	1	556					
K64	U	010000	1	557					
LCMT	H	000008	2	612					
MB	U	100000	1	558					
MSAAA	P	0009D0	8	566	465	468			
MSBEGCLK	D	0009A8	8	562	398	406	419	429	
MSDUR	D	0009B8	8	564	430	463			
MSENDCLK	D	0009B0	8	563	404	428			
MSG	I	000898	4	495	212	245	278	297	477
MSGCMD	C	0008E2	9	521	508	509			
MSGMSG	C	0008EB	95	522	502	519	500		
MSGMVC	I	0008DC	6	519	506				
MSGOK	I	0008AE	2	504	501				
MSGRET	I	0008C8	4	515	512				
MSGSAVE	F	0008D0	4	518	498	515			
MSOVER	D	0009A0	8	561	407	464			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
SKL0003	U	00004E	1	260	276
SKLF14	U	000051	1	304	295
SKPWS	X	0004C0	8	308	287
SKT0001	C	000232	20	191	194 211
SKT0002	C	0002DC	20	224	227 244
SKT0003	C	00038C	20	257	260 277
SVOLDPSW	U	000140	0	127	
T1	A	000AF8	4	718	2388
T10	A	000EE8	4	952	2397
T11	A	000F58	4	978	2398
T12	A	000FC8	4	1004	2399
T13	A	001038	4	1030	2400
T14	A	0010A8	4	1056	2401
T15	A	001118	4	1082	2402
T16	A	001188	4	1108	2403
T17	A	0011F8	4	1134	2404
T18	A	001268	4	1160	2405
T19	A	0012D8	4	1186	2406
T2	A	000B68	4	744	2389
T20	A	001348	4	1212	2407
T21	A	0013B8	4	1238	2408
T22	A	001428	4	1264	2409
T23	A	001498	4	1290	2410
T24	A	001508	4	1316	2411
T25	A	001578	4	1342	2412
T26	A	0015E8	4	1368	2413
T27	A	001658	4	1394	2414
T28	A	0016C8	4	1420	2415
T29	A	001738	4	1446	2416
T3	A	000BD8	4	770	2390
T30	A	0017A8	4	1472	2417
T31	A	001818	4	1498	2418
T32	A	001888	4	1524	2419
T33	A	0018F8	4	1550	2420
T34	A	001968	4	1576	2421
T35	A	0019D8	4	1602	2422
T36	A	001A48	4	1628	2423
T37	A	001AB8	4	1654	2424
T38	A	001B28	4	1680	2425
T39	A	001B98	4	1706	2426
T4	A	000C48	4	796	2391
T40	A	001C08	4	1732	2427
T41	A	001C78	4	1758	2428
T42	A	001CE8	4	1784	2429
T43	A	001D58	4	1810	2430
T44	A	001DC8	4	1836	2431
T45	A	001E38	4	1862	2432
T46	A	001EA8	4	1888	2433
T47	A	001F18	4	1914	2434
T48	A	001F88	4	1940	2435
T49	A	001FF8	4	1966	2436
T5	A	000CB8	4	822	2392
T50	A	002068	4	1992	2437
T51	A	0020D8	4	2018	2438
T52	A	002148	4	2044	2439
T53	A	0021B8	4	2070	2440

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	10256	0000-280F	0000-280F
Regi on		10256	0000-280F	0000-280F
CSECT	ZVE7TST	10256	0000-280F	0000-280F

STMT	FILE NAME
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```
1 /home/tn529/sharedvfp/tests/zvector-e7-99-performance.asm
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**** NO ERRORS FOUND ****